4. ERICSSON DXX MIDI NODE

4.1 General

The Ericsson DXX Midi Node is a flexible access node for customer premises. It offers the same cross-connect functionality as a Basic Node (64 Mbit/s) in a cost-efficient package. The heart of the Midi Node is a one-slot wide multifunctional interface unit, the XCG, which combines the functions of a cross-connect unit and a control unit. In addition, it provides four 2 Mbit/s G.703 interfaces, either 75 or 120 ohms. The DXX Midi Node supports the same interface cards as the Basic Node, except for the GMU (SDH Interface unit) and FRU (Frame Relay Unit). Trunk interface units, customer access interfaces, and server units can easily be added because of the modular structure of DXX nodes.

The Midi Node subrack (RXS-S8) consists of 8 slots (40T). A tabletop version (RXS-S8-TT) is also available.

4.1.1 Interface Types

There are numerous combinations of interface options on the DXX Midi Node. The modular structure of units and nodes enables flexible expansion of the DXX system. For a list of available unit and module combinations, see page 25 .

Trunk Interfaces

Type	Interface Unit
8448 / 2048 kbit/s	GMH
320 up to 4096 kbit/s	GMH
n * 64 kbit/s (n=2…32)	GMH
1544 kbit/s (T1)	GMM
2048 kbit/s	XCG

User Access Interfaces

Type	Interface Unit
2048 kbit/s	GMH, GCH
600 kbit/s…2048 kbit/s	VCM
600 kbit/s…64 kbit/s	VCM
64 kbit/s	VCM
0 bit/s…64 kbit/s async	VCM

Other Interfaces

- CAE voice frequency and signalling interfaces
- POTS interface unit for telephony applications
- ISD-LT and ISD-NT network and line termination interfaces

Server Units

- EPS voice and fax compression unit
- EAE ADPCM server unit, ADPCM compression
- ECS V.110/X.50 conversion unit

4.1.2 Technical Data

Cross-Connect Functionality

Fully non-blocking cross-connect capacity for Midi Node is 64 Mbit/s, which can, for example, be allocated as 32 x 2 Mbit/s or 8 x 8 Mbit/s.

Special Functions

Path protection: The Midi Node supports 1+1 path protection. Trunk and circuit level recovery by NMS.

Broadcast: unidirectional broadcast circuits are easily configurable via the NMS.

Point-to-multipoint: with a server card in the Midi Node, the system supports point-to-multipoint functionality.

Network Management System (NMS)

The Midi Node is totally manageable and configurable with the Ericsson DXX Network Management System. NMS release 9.0B or later is required.

Alarms

In PFU-A four alarm contacts are accessible through the D-type, 9-pin male connector on the front panel.

Operating Temperature and Humidity

Normal conditions. + 5° to +35° C, from 5 per cent to 85 per cent non-condensing.
Exceptional conditions: - 5° to + 45° C, from 5 per cent to 90 per cent non-condensing.

Power Supply Options

Each Midi Node must be equipped with common units, which are the power unit and the system control and cross-connection unit, XCG. There is a number of power supplies available:

— PFU-A: DC power supply - 48 V and 24 V: 30…60 V, positive pole earthed, can be duplicated with PFU-B.
— PAU-5T: Slim AC power supply: 90…240 VAC, 47…63 Hz, can be duplicated.

Power Consumption

< 60 W, one Midi Node subrack equipped with 2 Mbit/s G.703 interfaces.

Physical Size (w x d x h)

Midi Node subrack (RXS-S8): 213.2 x 265.8 x 190.3.
Tabletop casing: 244 x 321 x 353 mm.
Plug-in units: 25 x 160 x 233 mm (5T), 50 x 160 x 233 (10 T), 75 x 160 x 233 (15 T).
Weight: < 10 kg Midi Node subrack including units.

4.2 Midi Node Common and Interface Units

4.2.1 General

Common units required in a Midi Node are the power supply unit PAU-5T and a cross-connect and control unit XCG. Descriptions of the interface and server units follow the description of the XCG unit.

- GMH
- VCM
- GCH-A
- CAE
- AIU
- CCO and CCS
- GMM
- VMM
- ISD-LT/ISD-NT
- IUM-5T/IUM-10T
- EAE
- EPS
- ECS
- PMP

4.2.1.1 Unit Mechanical Installation

The units of a DXX cross-connect node have modular structure. The design utilizes a standard base unit shown in the figure below. The main parts of the base unit are:

1. Main unit with base mechanics (EMC shields) and two euro connectors, which connect the unit to the motherboard of a subrack.
2. Interface modules. A typical interface unit comprises two interface modules. A module includes its own front panel (EMC shield) without any text.
3. Unit power supply module PDF.
4. Front panel assembly.
5. Fastening screws for front panel.
6. Fastening bar.

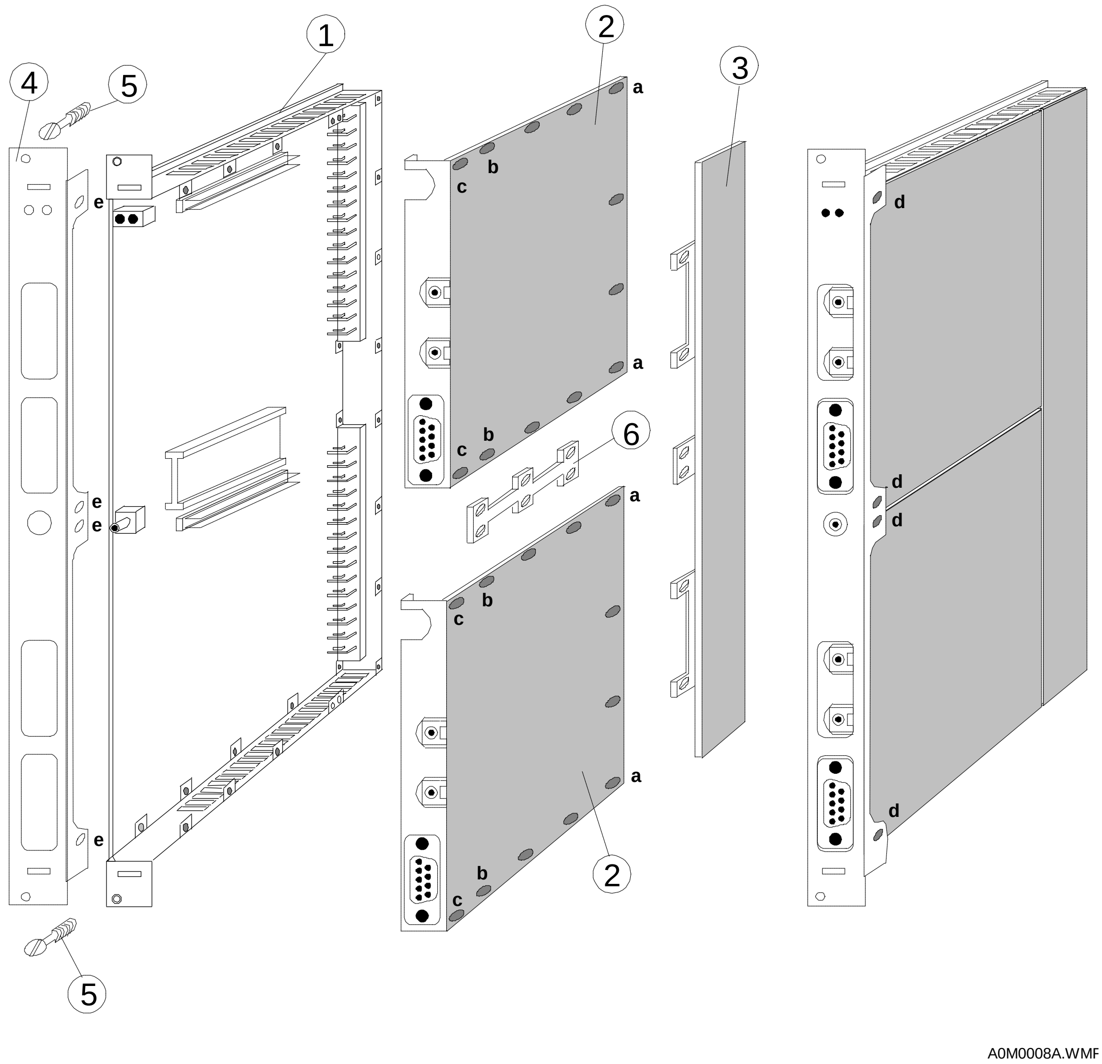


Fig. 1: Main Parts of the Base Unit

M2.5x4 (shorter) and M2.5x6 (longer) screws are delivered with the unit. The modules are fastened to the main unit with M2.5x4 screws and the front panel is fastened to the unit with M2.5x6 screws.

In most cases the power module is already fastened to the main unit in the factory.

The following steps are required to assemble the interface modules and front panel:

NOTE! ***When installing modules, take care not to scratch the surface of the printed circuit boards and not to bend any components or their legs.***

Step 1. Check that the strappings of the interface modules are correct for your application. Strapping instructions are given in chapter Strapping Instructions.

Step 2. First take the module which you want to install to the upper module position.

- Fasten the fastening bar to the bottom of the module (the side where the components are) with three short screws.
- The screws are secured in the three holes in the middle of the module.
- Do not fasten the screws tightly yet because the bar should move a little to help the installing of the screws of the lower module.
- When the unit is ready, the bar connects the interface modules together and is a part of the EMC shield of the unit.
- In the figure above the fastening bar can be seen in the middle of the unit between the interface modules.

Step 3. Install the upper module on the main unit.

- The pin connector of the main unit near the LED holder should go into the connector near the upper edge of the interface module.
- When connecting the interface modules to the pin connectors, do not to bend the pins of the connectors.
- Check very carefully that the pins are set into the connectors in the correct position.
- Check that the screw holes of the main unit are exactly on the screw holes of the interface module.
- The gap between power module and the back edge of the interface module should be about 0.1…1.0 mm.

Step 4. Install the lower module on the main unit.

- The pin connector of the main unit near the measurement connector and the EPROM should go into the connector near the upper edge of the interface module.
- Do not bend the pins of the connectors.
- Check very carefully that the pins are set into the connectors in the correct position.
- Check that the screw holes of the main unit are exactly on the screw holes of the interface module.
- The gap between the power module and the back edge of the interface module should be about 0.1…1.0 mm.

Step 5. There are now two interface modules on the main unit. Secure the fastening screws of the modules.

- Start with the shorter (M2.5x4) screws. Secure them on the corners of the modules near the power module: in the fourth hole from power module on the upper and lower edge of the unit. (Holes labelled a in the previous figure).
- Do not secure the screws nearest to the front edge of the unit because they are reserved for fastening the front panel. (Holes labelled c in Fig. 1).

Step 6. When tightening the screws, do not use too much force.

Step 7. Secure the fastening screws of the fastening bar on both modules.

Step 8. Secure the rest of the fastening screws starting from the left side of the unit; see figure above, beginning from holes a towards holes b.

- There should be 20 screws for the modules tightened now.

Step 9. Turn the unit left side up.

- There are eight holes near the front edge of the unit. Four of them are used for module screws (Fig. 1 and below Fig. 2)
- The holes near the upper and lower edge and the two holes in the middle of the unit are for the front panel. Fig. 1, hole d.
- Secure the module screws.

Step 10. The interface modules are now installed. Make sure that no loose parts are left inside the unit.

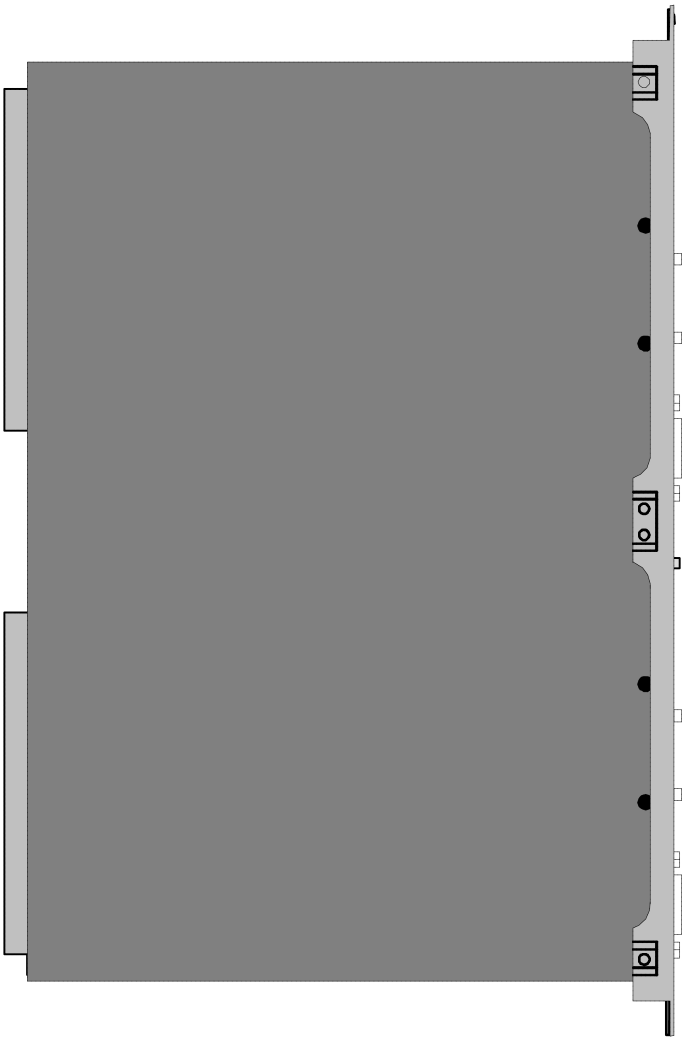


Fig. 2: Left Side of the Composed Unit

On the upper edge of the front panel there is the unit type text (GMH, for example), holes for the front panel screw, holes for out-pulling hook and two round holes for LEDs.

— Install the front panel carefully on the unit.
— Take care that the LEDs come correctly through the holes.
— If the modules are installed correctly, no screws are on the holes to fasten the front panel.
— If there are any screws in the holes reserved for the front panel (Fig. 1, hole d), remove the them and do not use too much force to push the panel on its place.

Step 11. Use the longer screws (M2.5x6) to secure the front panel.

— Secure four screws on both sides of the unit (eight altogether). The holes for the screws are on the upper and lower edge and in the middle of the unit. (Fig. 1, hole d).

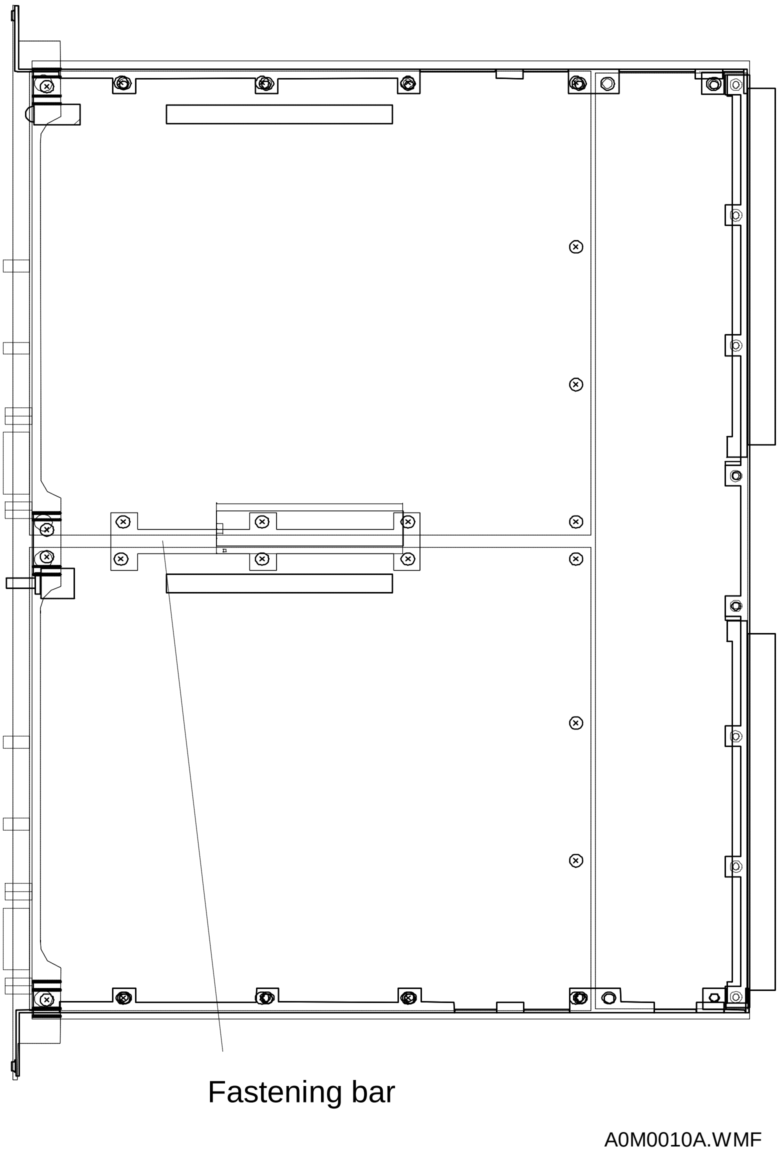


Fig. 3: Right Side of the Composed Unit

Step 12. The front panel screws are installed next.

- On the front panel assembly and in the frame of the unit are the holes for the front panel screws.
- The holes are the uppermost and the lowermost holes on the front panel.
- Screw the screws with fingers to their place. Do not use too much force or any tools to install these screws.

Step 13. On some units an insulation strip is needed. Add it according to the unit manual.

Step 14. The unit is now ready for use. Check that all screws are tightened and all parts and connectors are in good repair.

4.2.2 Power Supply Unit: PAU-5T

4.2.2.1 General

PAU-5T is a switchmode power supply. It has two DC output voltages, which are made from 90 - 264V AC mains voltage. The output voltages 48V and 5V are stabilized and galvanically isolated from mains.

The power supply has an active step-up type power factor correction which operates as preregulator for the actual converter. The PAU-5T is metal shielded 5T width unit and it has one output connector to subrack direction. It is intended for use in Midi subracks RXS-S8 and RXS-S8-TT if AC input is required. It can supply 80VA output power to subrack. It also supports protected power feeding.

CAUTION!

DISCONNECT THE UNIT FROM THE MAINS SUPPLY BEFORE REPLACING THE FUSES!

DOUBLE POLE/NEUTRAL FUSING!

Basically the PAU-5T unit contains the following parts Fig. 4:

1. PAU571 printed circuit board
2. cover plate
3. bottom plate
4. front panel
5. contact springs
6. power switch
7. fuse
8. front panel sticker (not in scale)

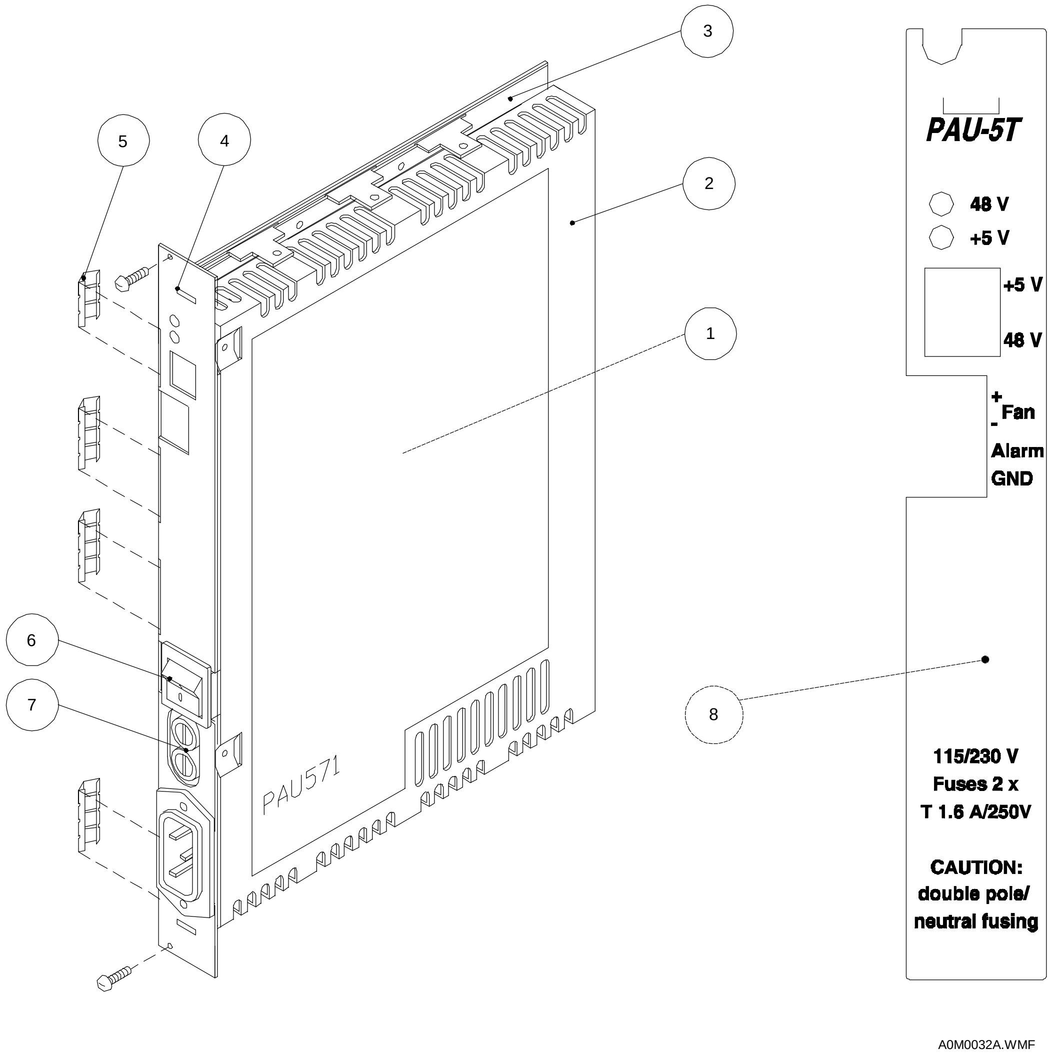


Fig. 4: PAU-5T Mechanical Structure and Front Panel Sticker

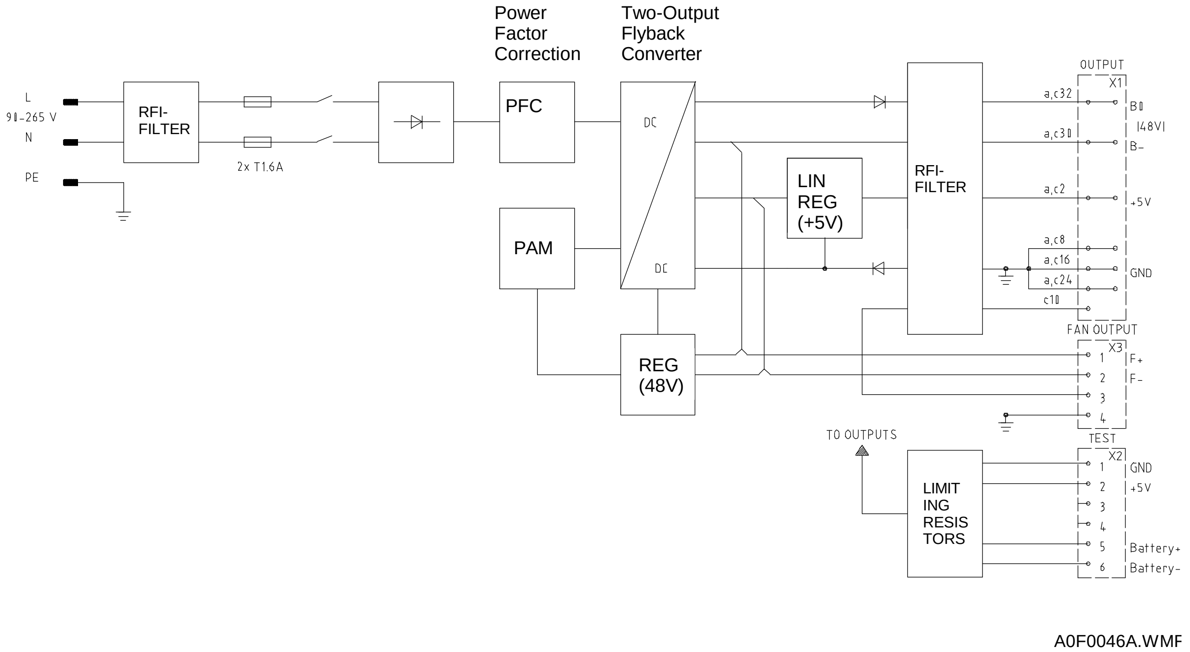


Fig. 5: Block Diagram of PAU-5T

The power supply input is protected against overcurrent with two fuses. Those are on the primary side (delay 1.6A fuse). An internal fault in the power supply may blow the fuses. The primary fuses can be replaced by opening the cap of the fuse holders in the unit´s front panel.

4.2.2.2 PAU-5T Block Diagram

General characteristics

The mains voltage from mains connector is fed through input filter and fuses to rectifier.

Input filter includes also the inrush current limit and over voltage protection. The rectified voltage is fed to power factor correction circuit (PFC). The PFC circuit forms a 400VDC voltage for power stage converter. The converter is a flyback type converter which forms the 48VDC output voltage. The pulse width modulation (PWM) circuit controls the power transistors and it protects the converter from short circuits and it starts automatically the normal operation after short circuit.

The feedback from output voltage is made via optoisolator.

The 5V output voltage is regulated.

The fan voltage output offers a 48V /100mA for an external fan if used.

PAU-5T Interfaces

The front panel of PAU-5T is provided with two indication leds, 48V and +5V, a connector output for external fan power and input for fan alarm, measurement points for 48V and +5V outputs, a mains switch, mains fuses and the mains input connector.

When the switch is in position 0 the mains voltage is disconnected from the converter.

4.2.2.3 PAU-5T Technical Specifications

Input specifications

Input Voltage	90…264V AC
Frequency range	47…63 Hz
Power factor corrector	Yes (>0,9)

Output specifications

Output voltage	48V DC	5.1V DC
Total output tolerance	< 10%	< 5%
Output current	0… 1.8A	0…0.5A
Maximum output power	80W	
Output difference (between separate units)	±- 5%	± 2%
Load regulation	± 5%	± 2%
Ripple voltage at switching frequency	0.5Vpp	50mVpp
Ripple voltage RMS 50MHz bandwidth	300mV	30mV
OVP	< 80V	< 7.5V
Hold up time	> 20ms	
Short circuit protection	Continuous with automatic restart	Continuous with automatic restart

Isolation levels

Input / Output	3.75kV AC
Input / Chassis	2.5kV
Output / Chassis	500V
Between outputs	500V

Environmental conditions

Environmental operating conditions: ETS 300 019-1-3; 1992- Class 3.1

Operation temperature / exceptional temperature	+5…+40 / -5…+45
Operation humidity / exceptional humidity RH	<85% / <90%

Dimensions

PCB size	160mm x 233.36mm
Front panel size	6U x 5T

4.2.3 Cross-connection and Control Unit XCG

4.2.3.1 General

The XCG is a highly integrated 5T wide unit combining the main functions of an SCU control unit and an SXU-A cross-connect unit. Additionally, a G703-75-4CH or a G703-120-4CH interface module can be installed on the XCG base unit. XCG has a cross-connection capacity of 64 Mbit/s. It cross-connects n x 64 kbit/s XB-channels with possible signalling (XD-channels) as well as a limited number of n x 8 kbit/s XB-channels. XCG is designed to operate as a part of DXX-network and can be controlled with Ericsson DXX Manager.

There are four G.703 2048 kbit/s E1 interfaces, synchronization input and output as well as Service Computer interface in the front panel of the unit. XCG consists of two cards, one XCG 525 base unit which contains control processor and cross-connection features and another GDH 521/522 containing E1 interfaces (IF1-IF4) and synchronization interfaces. Interfaces 1 and 2 can be used in 1 + 1 protected mode and they support full DXX trunk interface features including management via HDLC channel in any time slots or in the TS0 spare bits. Interfaces 3 and 4 do not support management HDLC channel and can only be used as user access point (UAP). IF1 and IF2 can also be used as UAP. All four interfaces can be used in framed or unframed mode. The frame structure of the interfaces is according to CCITT G.704. For more information about G703-75-4CH and G703-120-4CH interfaces see .

XCG consists of a base unit (XCG 525) and modules:

- PDF 202 (-48 V) or PDF 209 (+24 V) power supply module
- SMZ 538 unit software module
- G.703/G.704 (75 Ω) unbalanced interface module (GDH 521) or
- G.703/G.704 (120 Ω) balanced interface module (GDH 522)

XCG unit has modular structure. The XCG unit needs to operate one piggy-back power supply unit PDF 202 or PDF 209. The width of the unit is 5T or one card slot in DXX subrack. Card slot 8 in Midi Node is reserved for the XCG unit.

Starting from the upper edge of the front panel of the unit (G703-75 or 120-4CH equipped), there are two alarm LEDs, Service Computer connector, two G.703 interfaces, SYNC input/output connectors and again two G.703 interfaces. In the back of the unit there are two 2 x 32 pin eurocard (DIN 41612) connectors. The upper euro connector is used in transmitting the LOCAL VTP bus signals, equipment alarm output signals, 5 V power to the bus interface circuits and test input/output signals. The lower connector is used in transmitting the cross-connect bus signals, the 5 V power to the bus interface circuits and the battery bus. The power supply module is mounted on the base unit.

4.2.3.2 XCG Operation

XCG Block Diagram

The XCG unit takes care of subrack data and timing signals, 16896 kHz main clock of node, frame and multiframe synchronization signals. The external clock reference signal for the main clock can also be connected from any IF unit in the subrack as well as from the SYNC interface. One local VTP channel, subrack alarm output signals (PMA, DMA, MEI), node inventory management, storing parameters for all IF-units - excluding GMU and FRU units - in subrack and event reporting to the NMS are main responsibilities of XCG unit. XCG cannot be protected.

The functional block diagram is presented in Fig. 6. The common functional blocks are:

- Cross-connect block
- Microprocessor block for control functions
- Power supply PDF 202 or PDF 209
- Interface module G703-75-4CH or G703-120-4CH

The microprocessor block, the cross-connect block, and the data interface to subrack are located on the XCG 525 board, which is the main board of the unit. The channel interfaces and the sync-interface are located on the interface module.

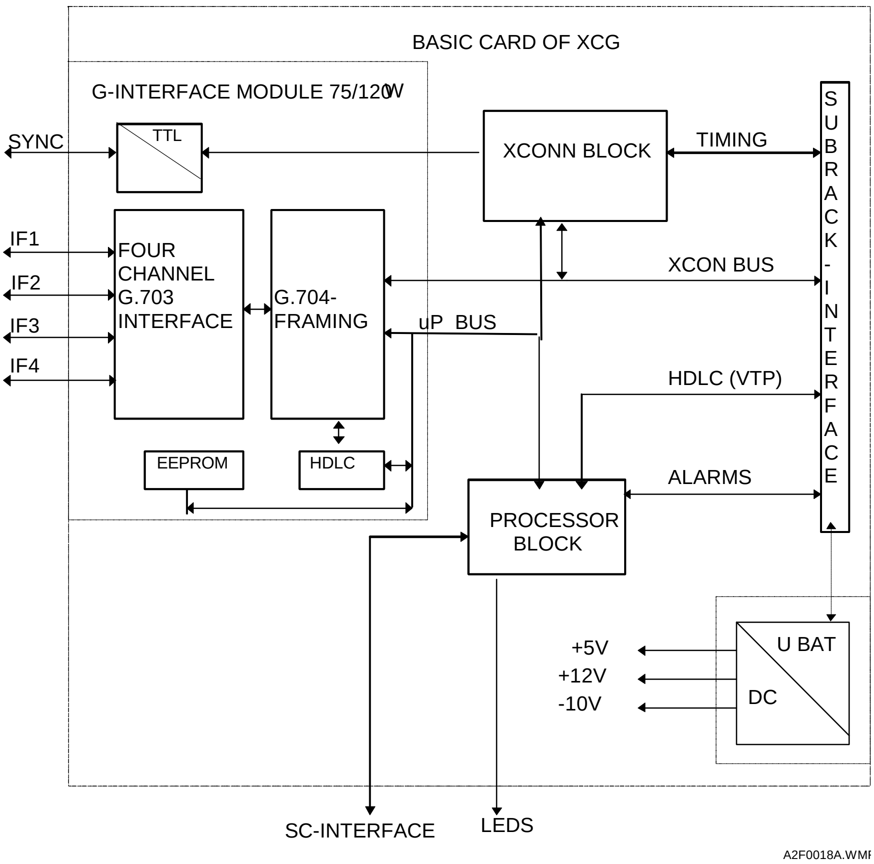


Fig. 6: XCG 525 Functional Block Diagram

Cross-Connect Block

The cross-connect block has the following main functions:

— cross-connection of data channels
— control of the cross-connect bus
— unit's master clock oscillator
— interface for external clock I/O
— selection of a reference signal for the master clock oscillator
— selection of a clock signal for the external clock output

The cross-connection is done in the switching matrix of the cross-connect block. The cross-connection bus contains 1056 cross-connectable time slots (8-bit bytes). The bits from the interface blocks are collected by using this bus. The cross-connect switch combines the needed new bytes for the interfaces by using 8 kbit/s granularity. Usually, whole time slots or bytes are cross-connected. The delay caused by the cross-connection is one 8 kHz frame (125 µs).

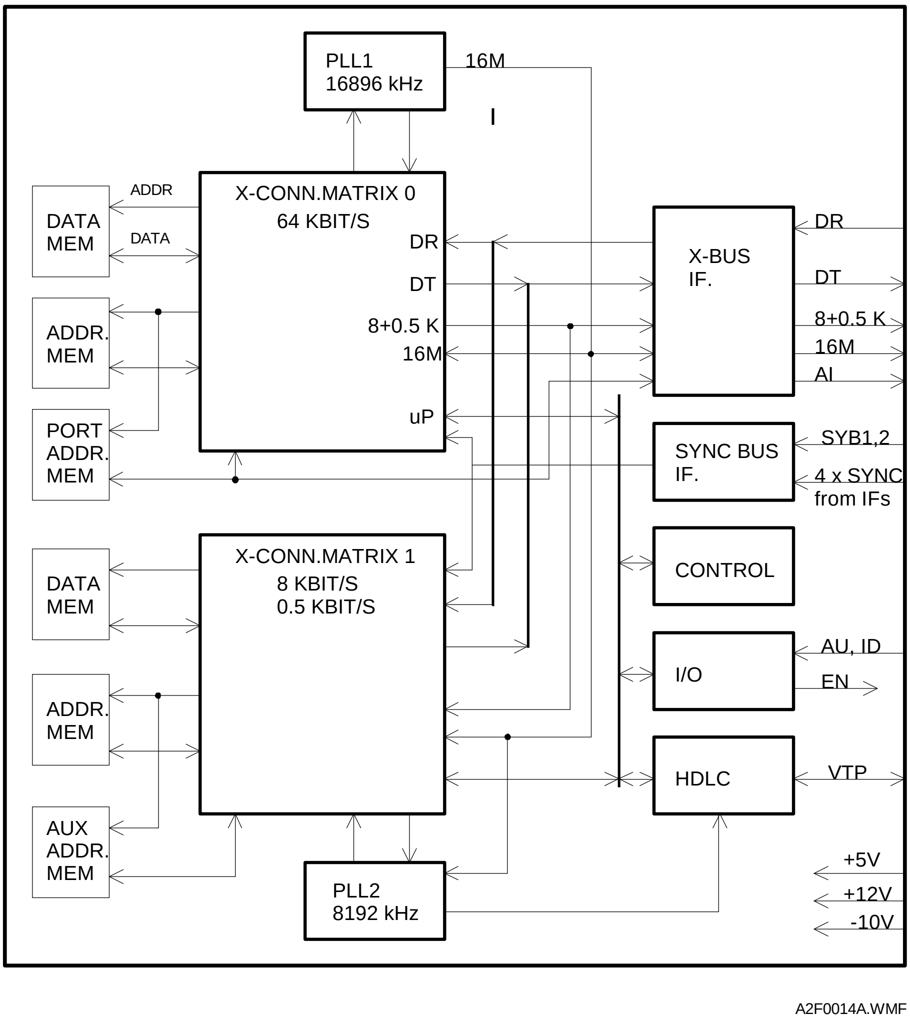


Fig. 7: The Block Diagram of XCONN block

The X-connect block exchanges data with IFs or IF-units by placing a channel address on the cross-connection bus, which activates data buffers of the corresponding channel. Rx & Tx data are carried on separate 8-bit buses.

The X-connect block supplies 16.896 Mhz master clock signal to the interface module and subrack. The Master clock is used to clock the bus operations and to create the correct frequencies for the transmitted signals.

XCG contains two cross-connect matrices (XCM) each handling distinctive connection types. XCG's software assigns tasks to the correct XCM.

Both XCMs enter the signal coming from the DR-bus into a buffer memory. Either of the XCMs outputs an octet in each cross-connected TSB to the DT-bus.

The cross-connect capacity of XCG is:

— 1043 x 64 (66 752) kbit/s of n x 64 kbit/s (octet) connections (total capacity).

Out of the total capacity can be allocated:

— 32 x 64 (2048) kbit/s to n x 0.5 kbit/s (channel associated signalling) connections and
— 95 x 64 (6080) kbit/s to n x 8 kbit/s (bit) connections

When calculating the capacity of a connection, add both ends of the connection to the capacity requirement; for example the two ports each in the example in section on page 18 require one 64 kbit/s octet.

Cross-Connect Matrix 0

XCM0 connects all n x 64 kbit/s XB-channels (fully non-blocking).

The DR-bus data is written into the buffer memory, which is two frames long, using an address from the frame counter. Data is read from the buffer with an address, which itself is read from a cross-connect address memory. The unit processor writes this cross-connect address when cross-connections are created.

In each cross-connected tsB a port address and a possible ts-address (framed interfaces) are read from a port address memory. The address is repeated in every frame. Several slow speed access interfaces in the same IF-unit can share a bus time slot, for example eight 8 kbit/s ports one tsB (subrate access interfaces at max. 4.8 kbit/s using a port rate of 8 kbit/s).

A number of ports can share an XD-time slot by using the same port address and activating themselves in only part of the frames.

XCM0 contains frame- and multiframe counters, which supply the X-bus timing. The frame- and multiframe counters of the XCM1 synchronize to the XCM0.

Cross-Connect Matrix 1

XCM1 provides n x 0.5 kbit/s XD-channel and n x 8 kbit/s XB-channel connections. Both types are connected bit-by-bit. Total capacity is 127 time slots (ts) per frame (8128 kbit/s).

Between 0 and 2048 kbit/s can be used for XD-channels (fully non-blocking). In XD-time slots the DR-bus signal is written into a two multiframes long buffer memory.

The maximum capacity for n x 8 kbit/s XB-channels is 95 ts per frame (6080 kbit/s). All ports in a node with XCG should be locked as uneven ports. Otherwise there may be blocking in the n x 8 kbit/s capacity.

XCM1 produces one cross-connected byte in every eighth tsB during the frame and transfers the byte temporarily into an internal buffer. All bits in a byte are processed even if some bits are not cross-connected (they are set to idle state '1'). Bytes are read from the internal buffer to the X-bus using addresses from an auxiliary address memory. XD-bytes are read from the buffer in tsB 528 to 559.

Microprocessor Block

The control microprocessor block contains the following functional units:

- Microprocessor
- Memory
- HDLC channel
- A/D conversion
- Service Computer Interface

Microprocessor

The unit is controlled with a 16-bit microprocessor. The processor has access to the cross-connect matrices and the cross-connect memories without interfering with the existing connections. A watchdog monitors the operation of the processor.The system program is stored on the board in two interchangeable EPROM memories. The application programs are stored in non-volatile FLASH memories; it is thus possible to update these programs from NMS. The non-volatile memory is also used to store the unit's operating parameters, the unit serial number, cross connection data info, port parameters and the parameters of all IF units in the node. In the case of a power interruption the unit is automatically reset to the conditions prevailing before the interruption, without specific parameterization. The RAM memory of the processor operates as a working storage containing e.g. error counters and data buffers for the HDLC links and the frame control bus. The microprocessor supports system-level testing.

Memory

The 512 kbyte non-volatile memory is for saving cross-connection data and port parameters as well as program code. Cross-connections can be repeatedly deleted and entered without capacity overflow. The core of the program code is stored in an EPROM. Memory is implemented with surface mount components.

- 256 kBytes RAM
- 512 kBytes Flash memory
- 256 kBytes of EPROM

HDLC Channel

The XCG unit processor links to the subrack control bus via an HDLC-controller. The XCG stores cross-connection commands and port parameters of IF-units in a non-volatile memory. The unit restores its state should a power loss occur.

A/D Converter

The unit includes a multichannel analog-to-digital converter (ADC) which monitors the operating voltages, auxiliary voltages 1 and 2 of subrack and control voltage of the master oscillator.

Service Computer Interface

The XCG unit has a single asynchronous serial channel. This interface is used on service computer connection (CNF1). The baud rate of the UART is 9600.

Power Supply

The unit receives its operating voltage from the power supply module. There are two models of power supply available, PDF 202 for -48 V battery input and PDF 209 for +24 V battery input. The modules can be replaced as a whole and plugged into the unit with connectors. The module is fixed with screws in a place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. The module provides the operating voltages +5V, +12V and -10V. The module also receives a +5V bus voltage, which during start-up conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset circuit and a low operating voltage results in unit reset. All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D converter. An alarm is generated if a voltage exceeds its limits.

Interface Module

Four-channel G.703 interface module is intended to be used with a XCG base unit. There are two alternatives of the unit, one for a 75 Ω unbalanced interface, G703-75-4CH and another for a 120 Ω balanced interface, G703-120-4CH. The modules include four independent E1 transmission channels to carry data and also to provide an internal communication link of the DXX system. The function of the module is to convert signals received by XCG base unit of a DXX node so that they comply with G.703 specifications and other relevant recommendations concerning the electrical interface towards equipment outside the DXX network. The G703 module also converts signals from other equipment into signals acceptable to the DXX network. Transmission channel interfaces are independent of each other. The frame structure is in accordance with G.704 for 2048 kbit/s. Two interfaces can be used for DXX trunk connections with a 1+1 protection possibility and all four interfaces can be used as user access points. See chapter G703-75/120-4CH Interface Module for details.

Internal Buses

Cross-Connect Bus Structure

Cross-connect bus functions are also monitored by the interface units. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm, if it cannot receive its channel address from the bus. The interfaces monitor the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing the interface unit will activate the Bus Sync Missing alarm.

XCG is continuously testing the XCON bus by transmitting test patterns in TS 1053.

The cross-connect bus covers unit positions 2 to 8 in the Midi Node.

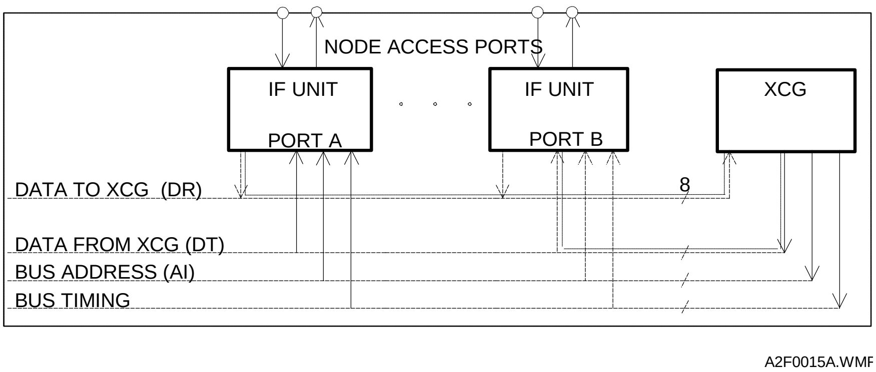
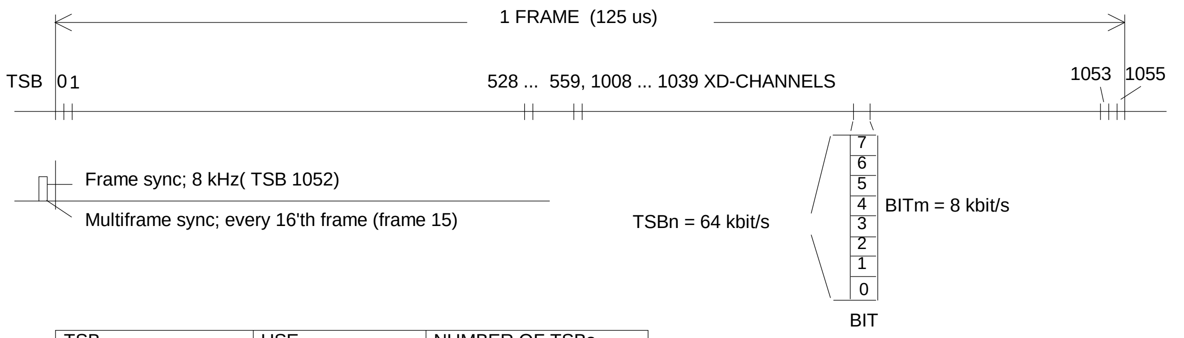


Fig. 8: X-Bus Signals

The X-bus operates synchronously. Interface units (IF-units) adjust mesochronous or plesiochronous access port signals into the X-bus by bit buffering. IF-units with a frame structure also buffer the frame (multiframe) phases.

XCG supplies the bus clock (16896 kHz), frame timing (8 kHz) and multiframe timing (0.5 kHz). XCG generates a port address for each cross-connected bus time slot. A port exchanges a data byte with XCG when the port recognizes its address. Ports with a frame structure receive the frame time slot number explicitly.



TSB	USE	NUMBER OF TSBs
0,1	BUS TEST	2
2 TO 9	UNUSED	8
10 TO 527	XB-CHANNELS	518
528 TO 559	XD-CHANNELS	0 TO 32
560 TO 1007	XB-CHANNELS	448
1008 TO 1039	XD-CHANNELS	0 TO 32
1040 TO 1052	XB-CHANNELS	13
1053 TO 1055	BUS TEST	3

TSB = BUS TIMESLOT

A2F0007A.WMF

Fig. 9: Logical Structure of the X-Bus

The X-bus frame is divided into 1056 bus time slots (tsB) numbered from 0 to 1055. Each tsB has a capacity of 64 kbit/s. Each of the eight bits in a tsB can be considered as a separate 8 kbit/s channel. Up to 32 tsBs can be further multiplexed by the 16 frames long multiframe for XD-channel cross-connection. The XD-time slots are cross-connected bit-by-bit creating n x 0.5 kbit/s channels.

Five time slots are reserved for node monitoring. The remaining 1051 bus time slots are reserved for cross-connection of user data.

X-Bus Allocation

X-bus capacity is allocated by the XCG software based on selected port parameters. Ports are classified as even and uneven ports. XCG supports uneven allocation. 2048 kbit/s ports get an uneven allocation if receive buffer is 4 or 8 frames. An uneven port does not reserve tsBs for XB-channels until the time slots are cross-connected. A possible XD-time slot is reserved when the port is locked. More than 32 uneven 2048 kbit/s ports can be accommodated in a node, if part of the time slots are not cross-connected and if the signalling capacity is not limiting.

An Example of the Signal Cross-Connection Procedure

64 kbit/s XB-Signal Connection

The following sequence details the procedure when XCG cross-connects a byte between two 64 kbit/s ports. Fig. “: X-Bus Signals” on page 18 shows the data path in the direction from port A to port B (dashed line).

When the operator locks the port parameters the port is automatically allocated one tsB. The operator creates a cross-connection between the two ports.

In each bus frame for ports A and B:

— XCG outputs the port's address on the address bus
— XCG reads a cross-connect address from an address memory and using the address reads a data byte from the data memory
— The port and the XCG exchange a data byte
— XCG writes the byte it received into a data memory
— The port sends the byte it received to the access interface. The delay of XB-channels in the XCG is one frame (125 µs). The total delay through a node also includes the buffer delays in the IF-units.

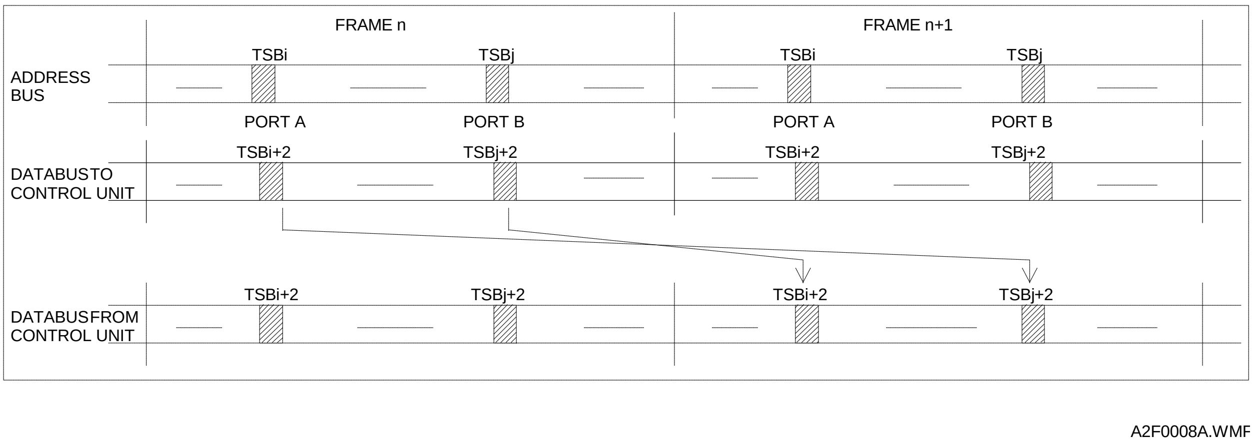


Fig. 10: Data Byte Exchange on the X-Bus

8 kbit/s XB-Signal Connection

The data exchange on the X-bus is similar to that of the 64 kbit/s signal. A whole byte is always transferred. XCG assembles the byte bit-by-bit during eight consecutive time slots. Bits, which have not been cross-connected, are set to idle state '1'. Signal delay is one frame within the XCG.

0.5 kbit/s XD-Signal Connection

The procedure is similar to the 8 kbit/s connection, but here the multiframe structure is employed. The delay in the XCG is one multiframe (2 ms).

X-Bus Interface

XCG supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the subrack: it is used to create clock frequencies for the transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

XCG exchanges data with the interface units by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. From the XCG the base units receive the time slot address which directs the bus data transmission to one selected time slot at a time.

Mux/Demux

In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern, which the receiver will search for in the received serial data flow. When the receiver finds it, the frame alignment signal is synchronized and, therefore, able to extract the payload data channels and to map them into desired locations. The frame alignment signals repeated at regular intervals divide the transmitted data into frames which have a defined structure for each transmission speed. In the DXX system the frame repetition frequency is always 8 kHz so that frames of different length, i.e. frames containing a different number of bits, must be used for different transmission speeds. A multiframe is created when several consecutive frames are combined into a frame structure by using a second frame alignment signal which is repeated at a lower frequency. For instance, signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

A more reliable receiver synchronization is achieved when a CRC check sum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC check is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver, which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference in the results, then the received data block contains one or more errors. The CRC check can be made for a data block of one frame, or alternatively, the CRC check is made for a data block consisting of several frames which then form a multiframe structure.

The CRC check sum is used to check the reliability of the synchronization by counting how many error-containing blocks are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value, there is a great probability that the receiver is synchronized to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronization word and to abandon the so called simulating frame synchronization word.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC check sum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

The internal communication of the DXX network is based on HDLC channels which are added to the framed signals. The unit processor can transmit and receive messages to/from other nodes with a two-channel HDLC controller connected to both framed interfaces of the unit. Usually the messages are sent via the control bus to the other units where they are processed or through which they are sent to other nodes. The transmission speed of the HDLC channels can be selected within the limits of 4 kbit/s to 64 kbit/s, depending on the requirements and the available transmission capacity.

In addition to the frame synchronization words and the transmitted data channels, the frame structures also include some bits for which the recommendations have not specified any function or which are not used in the application in question. These bits can then be used for the internal information transmission of the system. A system or organisation can also specify the use of these bits for some internal functions. In the DXX system the function of these special bits is defined through the user interfaces.

The frame structures are described in Appendices.

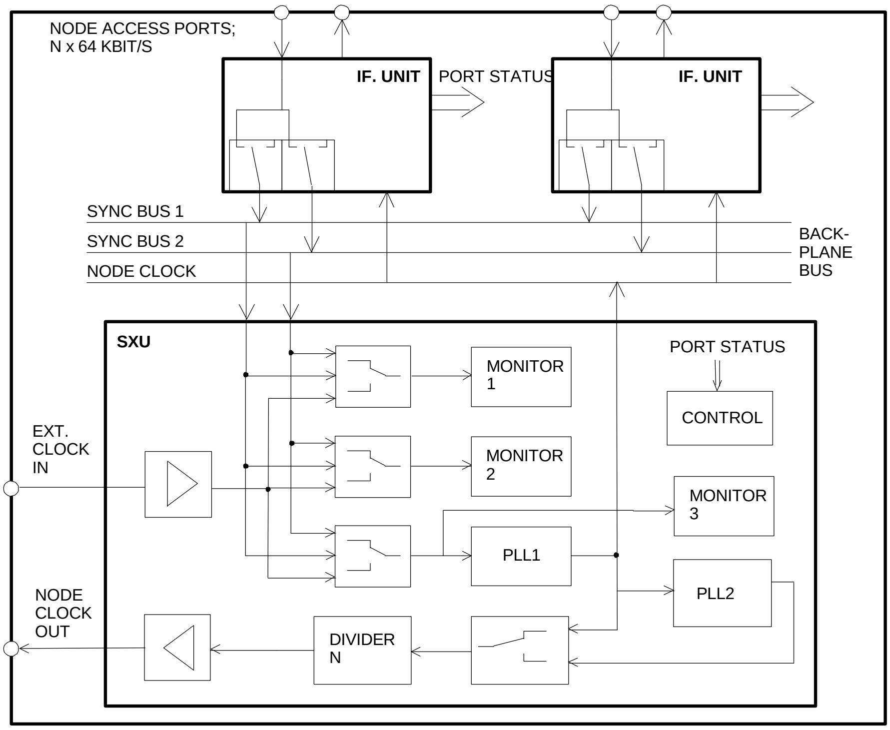
VTP Control Bus

The XCG unit has an interface for internal VTP control bus. The VTP bus is used for communication between the units within one subrack. The bus is synchronous serial high-speed local area network with data and clock lines and interface circuits. The bit rate of the local VTP bus is 2 Mbit/s.

VTP is an abbreviation from the words Virtual Token Protocol which is a collision-free media access method based on the token passing principle implemented by the aid of timers. The logical link control is based on LLC3 protocol in both buses. The upper layer protocols are the same as the those of the external management interfaces of DXX nodes. The local VTP bus supports unit addresses 1…31.

Node Clock System

The main oscillator (PLL1) runs at a frequency of 16896 kHz. Accuracy in internal timing mode is + 30 ppm over the operating temperature range. For jitter and wander specifications, see Chapter 4.2.3.5. The main oscillator can be locked to an external source or to the received clock of an access interface. Two synchronization buses are provided for transferring clocks to the XCG.



A2F0012A.WMF

Fig. 11: Node Clock System

Auxiliary Oscillator

An auxiliary oscillator (PLL2) is locked to the PLL1 providing frequencies in the 2048 kbit/s hierarchy for the clock output interface. Frequency of oscillation is 8192 kHz. PLL2 also supplies the 2048 kHz clock used for connection to the subrack control bus VTP and Tx-clock for GDH IFs.

Fallback List

In a DXX network trunk lines and the XCG’s external clock interface are normally used to transfer timing to the node. While the node clock can be synchronized from interfaces at lower rates (n x 64 kbit/s), it should be noted that synchronization from 2 Mbit/s and 8 Mbit/s signals results in better controlled wander properties.

The operator selects in the Master Clock-menu of the Node-window ports for the fallback list and assigns their priority. Up to five ports can be entered. The XCG selects the highest priority port with a non-alarm status as the input to the main oscillator.

Clock Monitoring and Alarms

XCG monitors the clock selected and also the next choice on the fallback list. The external clock is monitored when enabled.

Fallback list clocks are also monitored by the interface units. By a major fault in a port's rx-signal, the IF-unit clamps the clock (on SYNC BUS 1/2) and sends a clock status message to the XCG. XCG’s monitoring circuit opens the phase-locked-loop maintaining the clock frequency until the processor selects another clock. Internal timing is selected if all clocks on the fallback list have failed.

2 Mbit/s interfaces with a frame structure can employ a dedicated bit in the frame as a clock far end alarm bit (FEA). It is used on trunks transferring timing between nodes. If an intermediate node in a network loses its synchronization, the alarm bit is transmitted from all its interfaces. The receiving node’s IF-unit then clamps the clock on sync bus 1/2.

After a fault is cleared the IF-unit gradually clears the clock status. The operator can enter a clock acceptance time in the Master Clock-menu. A clock is not selected again until its status has been good over the acceptance time.

XCG supervises that the PLL1 is locked to the clock source. A phase-locked-loop alarm is generated if the source frequency is out of range or if it contains jitter more than specified in Technical Specifications.

Clock Output Interface

Node clock output is provided at the external interface in the XCG interface module (G703-75/120-4CH). The output is activated and its frequency selected from the Master clock window. The output control function, when set to on state, disables the output when the XCG is in internal timing or locked to the external interface. When output control is off, clock output is active regardless of the fallback list state.

Clock Faults Monitored in the XCG

Fault description	Status	Led	Alarm message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock on fallback list and missing	MEI	Red	Loss of external clock
External clock on fallback list, clock interface disabled	PMA	-	External clock warning
Locking to a clock failed	PMA	Red	Phase-locked-loop alarm
Main oscillator fault in XCG	PMA	Red	X-connect RAM fault
Clock far end alarm (individual for each link)	MEI	Yel	Clock far end alarm

If the node clock supplied by the XCG should fail, the GMH/GCH-units transmit an independent clock with a basic frequency tolerance to output ports. Node clock alarm is generated by the IF-units.

Node Level Operations

The software of the XCG takes care of the following node-level operations:

— Node Inventory Management

— Backup of unit settings
— Rack alarm (PMA, DMA, MEI) control
— Event reporting to the Network Management System
— Channel test loops

Node Inventory Management

The Node Inventory Management software includes functions to get and set node and subrack identifications, to create and delete inventory, to add and remove units, to get inventory reports and to monitor the presence of registered or unregistered units. The Create Inventory operation is used to register all existing units for the inventory. The Add Unit operation is used to register a given unit for the inventory. The Delete Inventory makes all units unregistered - in other words, all units are removed from the inventory. The Remove Unit operation is used to remove a given unit from the inventory.

The Inventory Report provides the node and subrack identification data and the list of existing or registered units. The Installation Error fault condition is detected if the inventory data is not unambiguous and consistent. The Missing Unit fault condition is detected if a registered unit is not present. The Extra Unit fault condition is detected if there is an unregistered unit present in the subrack.

Backup of Unit Settings

The XCG unit stores the backup settings of all registered units for possible unit replacements excluding GMU and FRU units. A new replacement unit will inherit the backup settings of the unit registered for the unit slot. The checking of compatibility of settings is based on hardware and software types.

The backup settings are updated to the XCG unit when a unit is registered or when the settings of the unit have been changed. The backup settings are copied from the XCG unit when a registered unit is replaced by another compatible unit (Chapter 4.3.4).

Rack Alarm Control

The XCG unit controls the three LEDs and the corresponding relay outputs for the equipment alarms (PMA, DMA, MEI) of a subrack. The rack alarm LEDs and the corresponding relay outputs are located in the PFU or PAU units. The rack alarms, PMA, DMA, MEI, are given if any unit in the subrack has an active fault condition which requires the corresponding alarm as a consequent action. The XCG unit collects PMAs, DMAs and MEIs from the units of the subrack and sums them separately for each rack alarm.

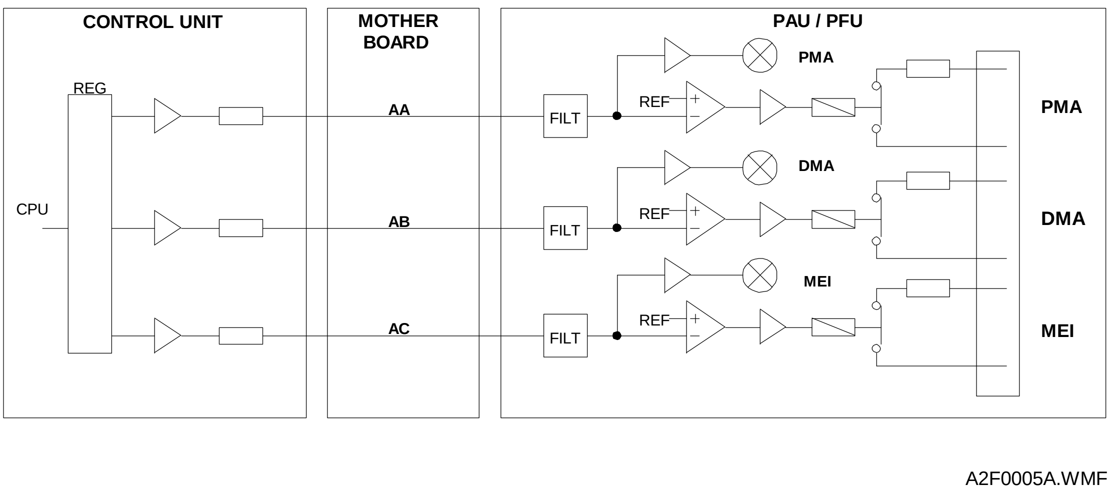


Fig. 12: Rack Alarm Control

Rack alarms can be delayed. The rack alarm delay can be set (0…600 seconds) by the user. A summed alarm must be active at least for the set delay time - not necessarily continuously - before the rack alarm is activated in PFU or PAU. The rack alarm will be passivated in PFU or PAU when the summed alarm has been continuously passive for at least the set delay time.

The rack alarm PMA and DMA can be cancelled. The rack alarm cancellation is not delayed. When PMA and DMA have been cancelled, MEI is activated as a reminder.

Event Reporting to Network Management System

The XCG unit does not only supervise the registered units of the subrack for the rack alarms but also to support subrack-level status polling from the centralized Network Management System as well. The node state report contains the status of the subracks which are not in the normal state.

The subrack state report contains the status of the units which are not in the normal state. For example, all changes in fault conditions and configuration are indicated for all units. These reports make it possible to get detailed information from the correct units for different purposes.

While the subrack state report is created, the route to the polling DXX server is updated to the local routing table of the XCG unit from the invoke message. This route can be used to send spontaneous event reports to the DXX Server. The unit reporting modules can send event reports to the local XCG unit which then sends them to the DXX Server. The most important application is the reporting of trunk fault changes in the trunk recovery management.

Interface Unit and Module Combinations

Midi Node can be equipped with several interface units which are used for external trunk and channel connections. These are application-specific depending on the trunk and channel requirements. Depending on the use of common units (control and cross-connection units and power units) and the redundancy requirements of the application, there are 4 to 6 interface unit slots available in a Midi Node Subrack RXS-S8. Node capacity is not determined solely on physical space, but memory and processor capacity must also be considered. The maximum cross-connect capacity of one Midi Node is 64 Mbit/s. This means that the total amount of bandwidth for the interface ports within one node cannot exceed 64 Mbit/s.

Interface units are used for line and user interfaces. Units are designed as single, double, or triple width cards, depending on their functionality. The actual DXX trunk and channel interfaces are defined by the interface module that resides as a subassembly on the base unit. Different kinds of interface modules can be mounted on the same base unit.

An XCG Multifunction unit equipped with G703-75/120-4CH interface module is an interface unit as well as a control and cross-connection unit for the whole Midi Node. Other available interface unit and module combinations for use in a Midi Node are listed below.

Interface Unit and Module Combinations

	Interface Units									
Modules	XCG	GMM	VMM	GMH	GCH-A	VCM-5T	VCM-10T	CAE	AIU 1:1	AIU 1:4
G703-75/120-4CH	x									
T1		x								
X21-G704-S			x	x						
V35-G704-BS			x	x						

	Interface Units									
Modules	XCG	GMM	VMM	GMH	GCH-A	VCM-5T	VCM-10T	CAE	AIU 1:1	AIU 1:4
V36-G704				x						
G703-75				x						
G703-120				x						
G703-8M				x						
OTE-LP				x	x					
OTE-LED				x	x					
LTE				x	x					
BTE-4096				x						
BTE-2048				x						
BTE-2048-2W				x						
BTE-1088				x						
BTE-384				x	x					
BTE-64					x					
V24-DCE						x				
V24-DCE-PMP						x				
V24-DTE						x				
V35-IEC						x				
X21						x				
G703-64						x				
V35							x			
V36							x			
PCM-10VF								x		
ADPCM-10VF								x		
EM-2*10								x		
STM-1-IO-13									x	x

In addition, the following interface units are available for Midi Node, but they contain no separate interface modules:

— IUM-5T
— IUM-10T
— ISD-LT/ISD-NT
— CCS-PCM
— CCO-PCM
— CCS-ADPCM
— CCO-ADPCM

Moreover, there are three server units which can be used in a Midi Node:

- ECS
- EPS
- EAE

G703-75/120-4CH Interface Module

General

Four channel G.703 interface module is intended to be used with XCG base unit. There are two alternatives of the unit: one for a 75 ohm unbalanced interface, G703-75-4CH and another for a 120 Ω balanced interface, G703-120-4CH. The modules include four independent E1 transmission channels to carry data and also to provide an internal communication link of the DXX system. The function of the module is to convert signals received by XCG base unit of a DXX node so that they comply with G.703 specifications and other relevant recommendations concerning the electrical interface towards equipment outside the DXX network. The G703 module also converts signals from other equipment into signals acceptable to the DXX network. Transmission channel interfaces are independent of each other. The frame structure is in accordance with G.704 for 2048 kbit/s. Two interfaces can be used for DXX trunk connections with 1+1 protection possibility and all four interfaces can be used as user access points.

Interface Module Operation

Mechanical Design

The mechanical design of the four-channel G.703 interface module is based on the standard DXX system mechanics. The module can be installed to an XCG base unit.

Operating voltage is fed to the module from the base unit through the same connectors that are used for signals for the control microprocessor bus and for the data transmission processing.

Power Supply

A module receives its operating voltage from the base module. The module requires the operating voltage of +5V.

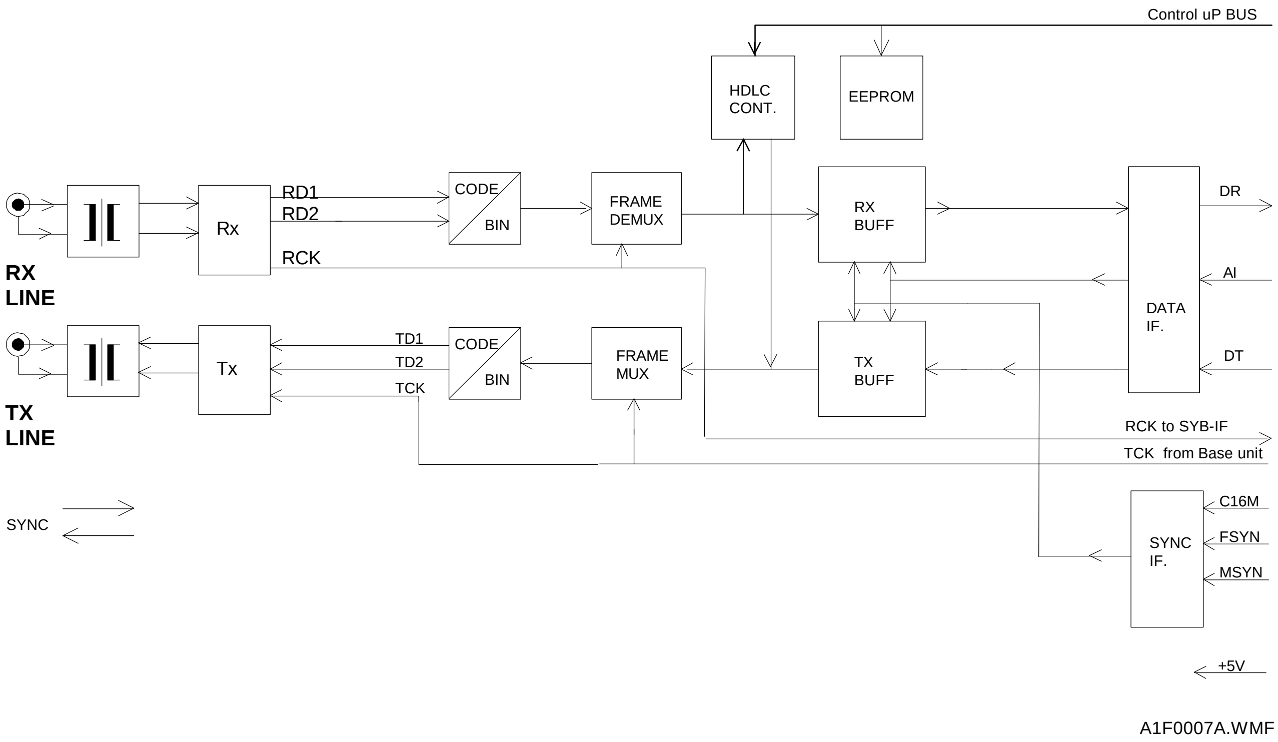


Fig. 13: Functional Block Diagram for one channel of the G703-75/120-4CH module

Control Processor bus

The interface module is controlled with a microprocessor located on the base unit. A non-volatile memory on the base unit is used to store the module's operating parameters so that in the case of a power interruption the module is automatically reset to the conditions prevailing before the interruption, without specific parameterization. EEPROM that is located on the module carries the serial number of the module, HW-version and module ID.

Line Interfaces

The four channel module is connected to a transmission line through interface circuitry. The block contains the analog components required for the E1 interface.

In the receiving direction the interface module regenerates the coded signal received from the transmission line and transforms the signal to the digital level. The module monitors the level of the received signal; if it is too low or completely missing, the module sets an AIS signal to the base unit and at the same time it activates a missing signal alarm through the processor bus. The behaviour is according to G.775.

Because the line interface provided by this module fully complies with all relevant recommendations, a complete specification of this interface is given under Technical Specifications only. The following briefly describes the line interface circuit design of the G703-75/120-4CH module.

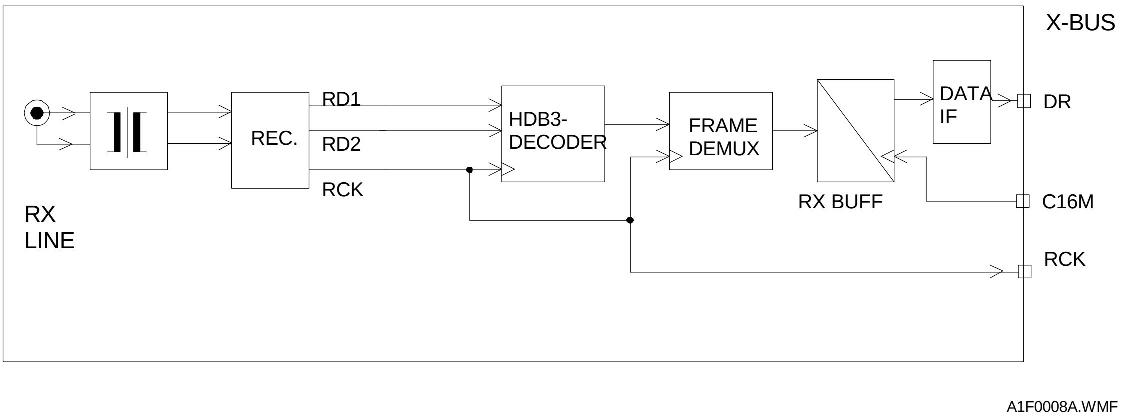


Fig. 14: Data and Clock Processing in the Receiving Direction

The receiving direction clock which is recovered from the data in the interface module is used to decode the line code and to demultiplex the frame. If there is no received signal, the interface module replaces the received clock with the transmitted clock.

The received clock from any of the four channels on the interface module can be connected to the two SYB buses on the base unit to be used as the node synchronization signal. The clock to the SYB-bus is disconnected if there is a received signal failure.

The module generates the frame structure and the G.703 line code for the data in the transmitting direction. The transmitting direction 2.048 MHz clock and C16M node clock received from XCG are phase-locked to each other.

In the Receive direction the line transceiver regenerates CMOS level RD1, RD2 and RCK from analog Rx signal. The input transformer together with resistors match the line impedance and amplitude for the line transceiver circuit. Diode limiters protect against overvoltage.

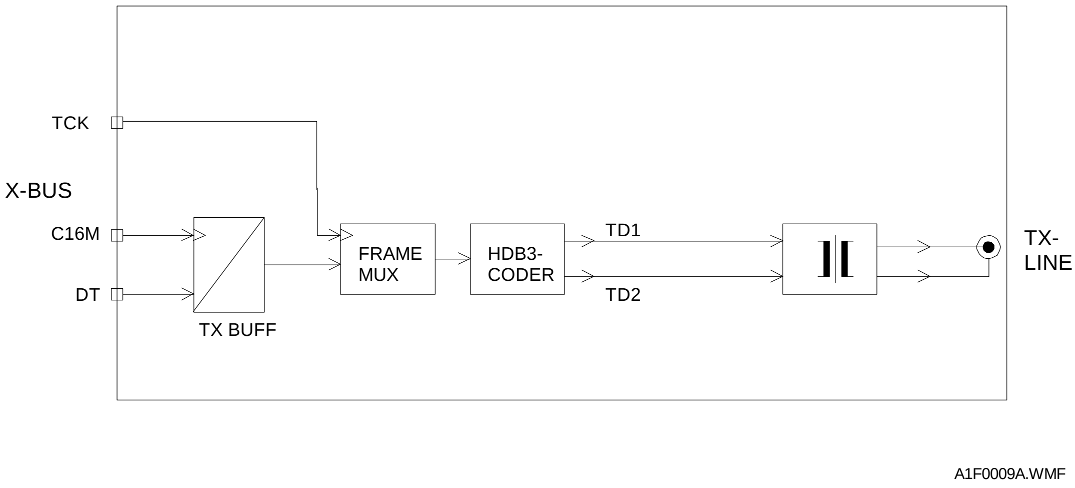


Fig. 15: Transmitting Direction Clock and Data Generation at 2048 kbit/s

The transmitting direction clock for 2048 kbit/s is generated by the crystal oscillator of the base unit. The oscillator is locked to the C16M clock of the bus, which is used to create the frame and to generate the output pulses in the coder.

In the transmit direction the CMOS level HI-active positive and negative pulses are fed to the line transceiver which produces pulse shape according to G.703 recommendation together with the line transformer and resistors. Output impedance matching to the line is also accomplished with the transformer and resistors. Diode limiters protect against overvoltage.

Clock Interfaces

An input interface for an external clock and an output interface for the node clock are provided. The interfaces comply with the ITU-T rec. G.703 § 10. Connectors that are the same type as the interface connectors are located in the front panel. For interface specifications Chapter .

Functional Structure

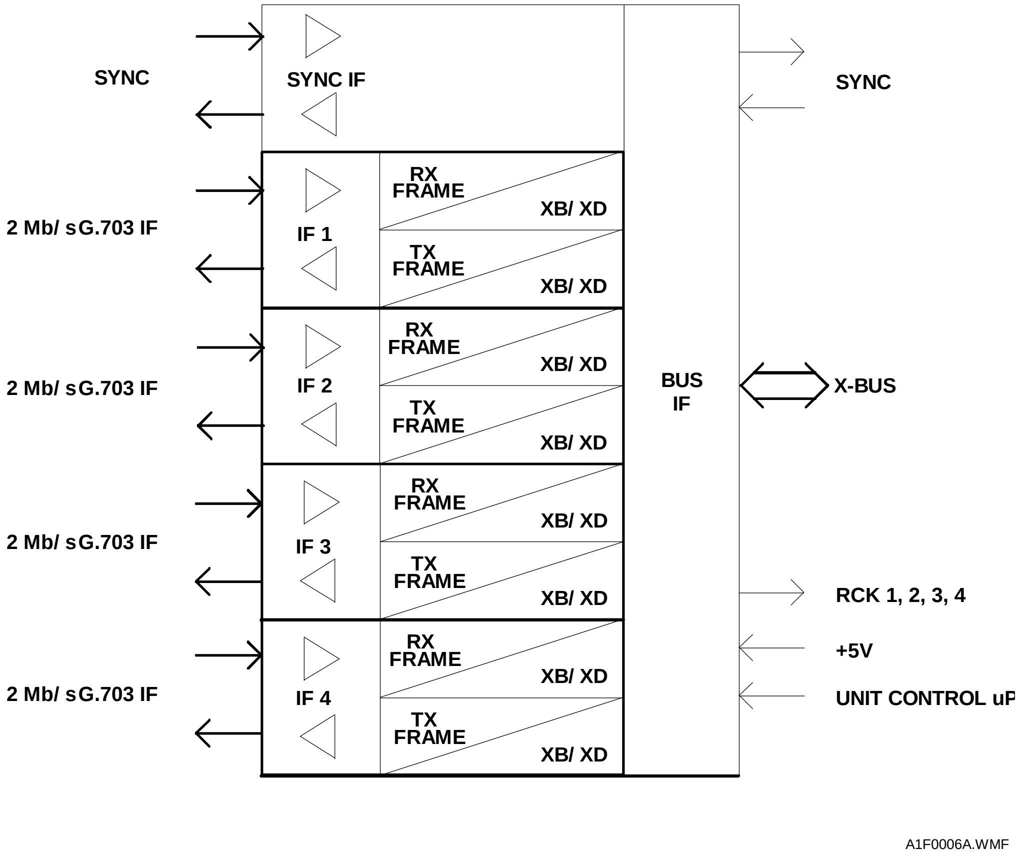


Fig. 16: Functional Structure of G703-75-4CH and G703-120-4CH modules

The main functional blocks of the G703-75-4CH and G703-120-4CH modules include line interfaces for four channels, channel frame multiplexer and demultiplexer circuits, channel output and input buffers, and an X-bus interface common for all channels.

The processor on the base module controls and monitors the functions of the interface module. Information related to control and monitoring is transmitted on an internal control bus of the subrack from the base unit. Through this control bus the base unit can communicate with other units in the subrack. The processor generates HDLC messages and processes HDLC messages received from framed interfaces.

The data transmission channel interfaces convert analog G.703 line signals to/from signals suited for the module's digital circuits. In the receiving direction a signal attenuated by the transmission line is regenerated and the clock signal is recovered. The payload signal and the clock signal are transformed to a level suitable for the digital logic. The line interfaces are realized at the same printed circuit board.

The framed signal which is carried on the transmission line is assembled and disassembled in the Tx-frame and Rx-frame blocks of each channel. In the transmitting direction the Tx-frame block creates a signal by mapping data from the X-bus into correct time slots, adding frame alignment signal bits and the CRC check sum, and by generating the HDLC channel at a required position within the frame, with the aid of the processor. Line transceiver converts digital Tx signal to analog signal at the line interface. In the receiving direction the line interface block converts analog signal to a digital signal. The Rx-frame block searches the received signal for the frame synchronization word. When the synchronization is found, the Rx-frame block can extract the data transmission time slots, check the CRC check sum, and recover and supply the HDLC channel to the processor. The frame structure is in accordance with G.704 / 2048 kbit/s. If required, it is also possible to remove the framing and have the channel to operate in a transparent mode.

The transmit buffers of the channels are used to store data received from the cross-connect through the X-bus, so that there is always a time slot available for transmit by the Tx-frame block. The transmit buffers also synchronize the phase of the transmitted frame with the phase of the X-bus and stuff idle data in unused time slots of the frame.

The receiving buffers of the channels store incoming data so that the required time slots are always available to the cross-connect module. These buffers also form a flexible buffer in order to compensate for minor momentary speed differences between the X-bus and the received signal. The length of the receiving buffers can be changed in accordance with the application's requirements. For instance, in some cases a minimum connection delay is required, and in plesiochronous operation slips are desired to occur as seldom as possible.

The X-bus interface transfers signals from the X-bus to the channels, timing signals and control information to the module, and correspondingly it transfers data and monitoring information from the channels to the X-bus.

X-Bus Interface

The base unit supplies the C16M clock for the interface module. The incoming C16M clock is also the central clock of the subrack: it is used to create clock frequencies for the transmitted signals. The base unit supplies frame alignment and multiframe alignment signals to the frame buffers.

The cross-connect unit exchanges data with the interface module by placing a channel address on the X-bus. This activates the data buffers of the corresponding channel of the interface module. Received and transmitted data is carried on separate 8-bit wide buses. Through the base unit the G703-75/120-4CH module receives the time slot address which directs the bus data transmission to one selected time slot at a time.

Bus functions are monitored by the interface module. When the interface is synchronized and the corresponding cross-connection is made, the unit will activate the IA Activity Missing alarm, if it cannot receive its channel address from the bus. When a unit is inserted and connected to the subrack, it monitors the combined information formed by the bus clock and multiframe synchronization signal; if this information is missing the unit will activate the Bus Sync Missing alarm. The Bus Sync Missing alarm inhibits the missing channel address alarm.

Mux/Demux

In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern, which the receiver will search for in the received serial data flow. When the receiver finds it, the frame alignment signal is synchronized and therefore able to extract the payload data channels and to map them into desired locations. A multiframe is created when several consecutive frames are combined into a frame structure by using a second frame alignment signal which is repeated at a lower frequency. For instance, signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

A more reliable receiver synchronization is achieved when a CRC check sum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC check is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver, which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference in the results, then the received data block contains one or more errors. The CRC check can be made for a data block of one frame, or alternatively, the CRC check is made for a data block consisting of several frames which then form a multiframe structure. The latter method is used by G703-75/120-4CH modules.

The CRC check sum is used to check the reliability of the synchronization by counting how many error containing blocks are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value, there is a great probability that the receiver is synchronized to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronization word and to abandon the so called simulating frame synchronization word.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC check sum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

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In addition to the frame synchronization words and the transmitted data channels, the frame structures also include some bits for which the recommendations have not specified any function or which are not used in the application in question. These bits can then be used for the internal information transmission of the system. A system or organisation can also specify the use of these bits for some internal functions. In the DXX system the function of these special bits is defined through the user interfaces.

The frame structures are described in Appendices.

Buffers

In the transmitting direction the buffer supplies time slot data from the X-bus to the frame to be transmitted. When the cross-connect unit supplies data to the X-bus, it also adds information about the location in the transmitted frame where the data is to be placed. The unit stores the data in its transmit buffer in a position corresponding to the time slot's position in the frame. The frame multiplexing circuits will fetch the data when they are transmitting the corresponding time slot. As it is possible to write the data from the bus to any time slot position in the buffer, the buffer must control that write and read operations do not simultaneously address the same time slot. In the G703-75/120-4CH modules the transmit buffer length is set to two frames. Then the frame multiplexing block reads the first frame area and the bus writes into the second frame area. This transmit buffer arrangement causes a delay of one frame or 125 µs.

In the receiving direction the buffer supplies received time slot data from the demultiplexed frame to the X-bus. When the XCG cross-connect block requests data from the interface module through the X-bus, it also specifies the time slot concerned. Usually, the phase of the received frame does not coincide with the frame phase of the X-bus; on the other hand, the receiver writes time slot data into the Rx buffer clocked by the received frame. Therefore the Rx buffer has to control that the read and write operations do not collide, in spite of speed fluctuations and jitter. If the read and write addresses come too close, one of them has to be moved, i.e. centred. The allowed minimum distance between the read and write addresses depends on the system requirements. In the interface module the centring is made by changing the read address, the change being always one frame or a multiple of a frame. The centring causes a certain number of frames to be lost or re-transmitted; the number is proportional to the distance which the read address is moved. Through the user interface it is possible to select four different lengths for the receiving buffer, in order to meet different requirements, such as a minimum delay or the ability to tolerate large speed fluctuations.

Centring is required when the equipment is powered up, when a received signal contains disturbances, or when the transmission is plesiochronous. If a plesiochronous system constantly exhibits a frequency difference in the same direction, the buffer has to be centred at regular intervals. The length of the interval depends on the frequency difference and on the distance from the centred read address position to the position where a new centring occurs.

Operating Modes of Buffers

Rx Buffer	Rx delay	Tx length	Tx delay
4 Fr	1…3 Fr	2 Fr	1 Fr
8 Fr	1…7 Fr	2 Fr	1 Fr

4 Fr Rx Buffer

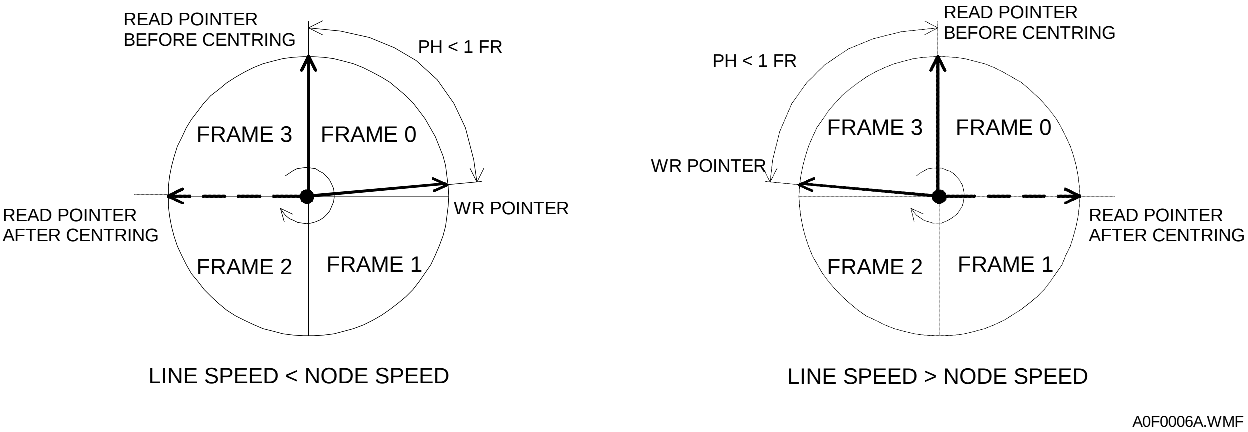

Fig. 17: Centring in an Rx Buffer of Four Frames

The minimum allowed distance between the read and write addresses is one frame. The distance is checked at intervals of four frames when the read address moves to frame Fr0 (from the frame Fr3). If the addresses are too close at the checking time, a centring is performed by moving the read address one frame further. The address jump direction depends on the direction from which the write address was closing in on the read address. Centring means here that one frame is either lost or repeated once. In a plesiochronous system with a four-frame Rx buffer the interval between centring situations is: at 2048 kbit/s 256/df.

8 Fr Rx Buffer

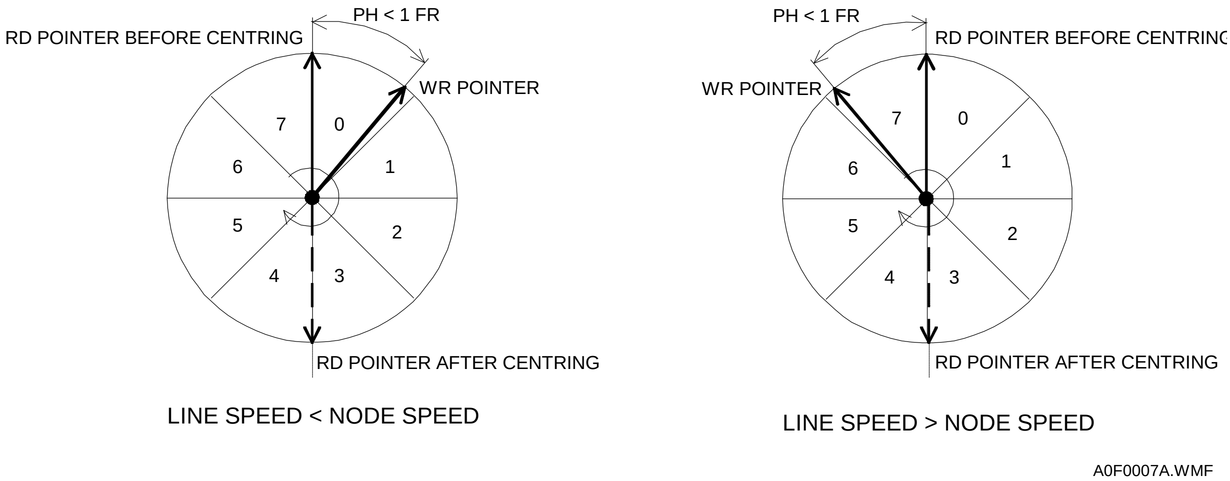

Fig. 18: Centring in an Rx Buffer of Eight Frames

The allowed distance between read and write addresses in an Rx buffer of eight frames is one frame. If a shorter distance is detected by the check, then the read address is moved to a new position four frames farther away. In this case centring means that four frames are either lost or repeated once. The eight frames buffer retains the frame alternation also after the cross-connect, when a 2048 kbit/s framing structure is used.

In a plesiochronous system the interval between centring situations is: at 2048 kbit/s 1024/df

Multiframe Buffers

In the transmitting direction the signalling data is directed through the same buffer as the time slot data. The signalling multiframe of the frame to be transmitted is synchronized to the multiframe clock of the X-bus. The cross-connect unit supplies frame signalling data together with other time slot data of the frame. The interface module generates a synchronization time slot in the first frame of the signalling multiframe. Thus the signalling data and time slot data have equal delays in the transmitting direction.

In the receiving direction the phase of the received signal multiframe usually differs from the phase of the X-bus multiframe. Thus the received signalling data has to be buffered until the cross-connect unit performs the cross-connect function for the concerned data.

Multiframe Buffers

Frame buffer mode[a]	Multiframe buffer mode[b]	MFr-Rx delay	MFr-Tx delay
4…8 frames	2 MFr	0…2 MFr	1 Fr

a The length of a frame is 125 μs.

b the multiframe length is 2 ms.

The centring is triggered if the distance between the received multiframe phase and the X-bus multiframe phase is less than one frame. In a buffer with two multiframes the centring is made by moving the write address one multiframe further, which means that the information of one multiframe is lost or repeated.

In interface module and cross-connect unit the time slot data and signalling data have separate buffers. Therefore there are different delays in the processing of signalling data and time slot data. This means that the signalling data and time slot data which are placed in a transmitted frame do not necessarily originate from the same frame.

G703-75/-4CH Interface Module Operating Modes

Trunk interfaces and user access interfaces are the two categories of DXX node interfaces. Trunk lines are lines connecting the DXX nodes, and the trunks are always framed interfaces. The interface module supports full DXX trunk features at interfaces 1 and 2. User access interfaces connect lines from users to a node. The user access interfaces can be channel interfaces or framed channel interfaces. The user interface presents a G.704 framed channel interface to the user. The most important difference between the trunk mode and the user mode is that the use of time slots in the trunk interface is determined by the Network Management System whereas the use of time slots in a framed channel interface is determined by the user. All interfaces on the module can be used as user access ports.

2048 kbit/s Trunk

When a line is used as a trunk line, a part of the frame is dedicated to transfer internal system information. This information will contain data on e.g. network management channels that use the HDLC format. The transmitter will always regenerate the frame synchronization word and the CRC check in a trunk line.

The framing and CRC check have to be selected when a trunk line connection is established. The corresponding HDLC channel has to be activated and bits B5…B8 in time slot ts0 are recommended bits for the link. The trunk buffer is short in order to ensure minimal delay through the node. It is recommended to activate the signalling time slot CAS of the trunk so that it is always reserved for signalling and not used as a data time slot by the Network Management System.

Split Trunk Lines

A split trunk line can be used to combine several parallel 2048 kbit/s interfaces in order to increase the maximum number of time slots of a n x 64 kbit/s trunk interface. The time integrity of the time slots in the split trunk line is preserved even if the 2048 kbit/s is connected through physically separated cables. The split trunk mode can be used when a frame with CRC4 is used. The split trunk mode always requires long buffers (eight frames). One of the interfaces will function as a master and the others as slaves. All split components must have the same bit rate.

The interfaces are synchronized to each other by their CRC4 multiframe structure. In the transmitting direction the interface transmit buffers and Tx-frame multiplexers are synchronized with the X-bus MSYN signal to transmit in the same multiframe phase. In the receiving direction the master interface sends information about its receiving buffer read phase to the slaves, which will center their own receiving buffers to the same phase. This operation causes data time slots sent from a transmitting node in the same frame to be read together within one frame into the cross-connect unit of the receiving node.

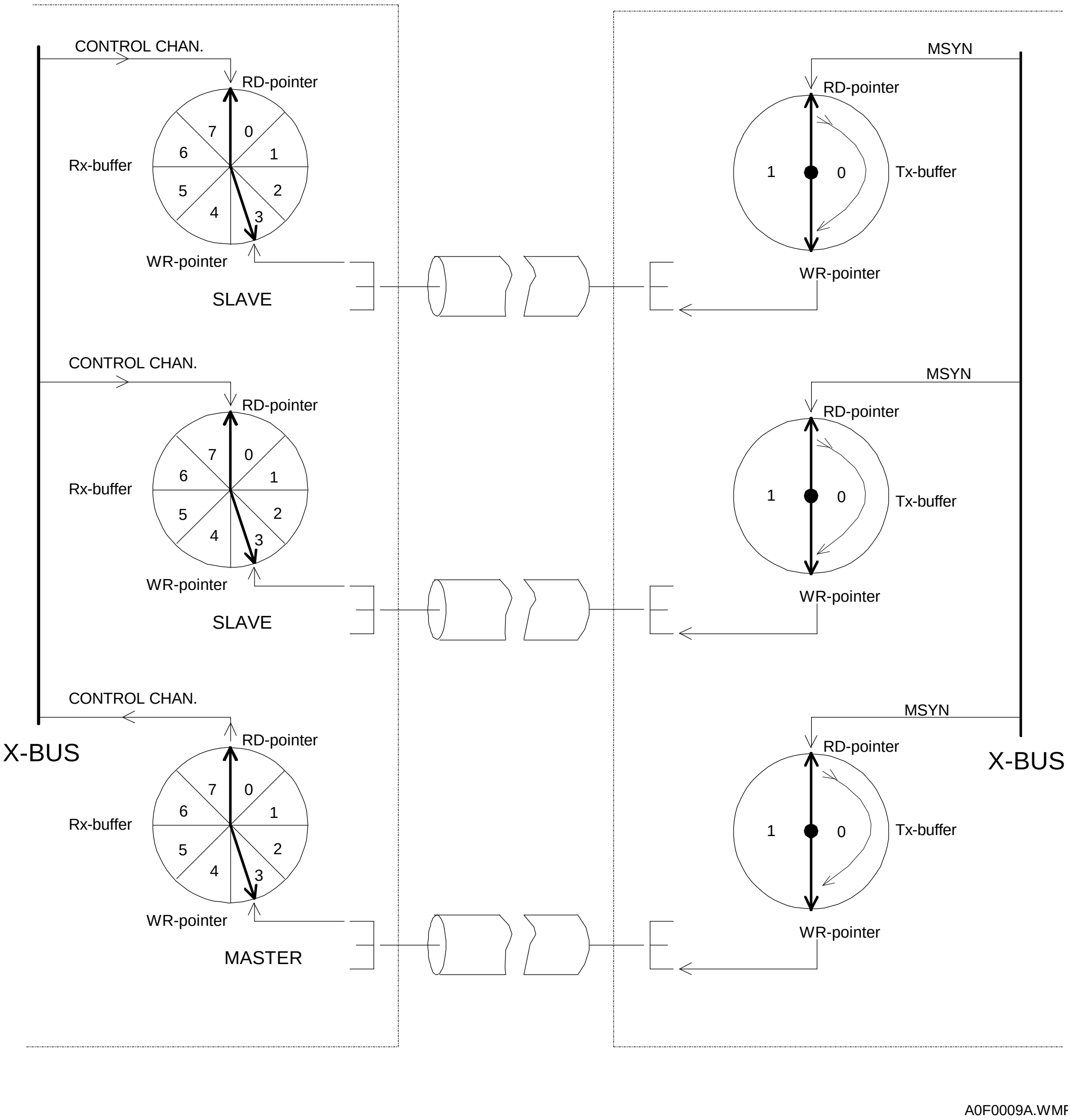

Fig. 19: Split Trunk Line Operating Principle

Theoretically, the maximum delay allowed between lines in a split trunk line is 0.5 frames: due to the centring the master read address occurs when the write address is in the area 6…2. Due to technical reasons, however, the maximum delay is 50 µs.

Each line of a split trunk line will handle its own signalling data. Those lines which carry one or more data channels with signalling data will use the last time slot or ts16 if it is possible as a signalling channel with a multiframe structure. It is not necessary to use a CAS time slot for lines that do not include data channels with signalling.

Interface module as User Access Point

The interface module can provide a G.704 framed channel interface to the user. The framed user access point has the same features as a corresponding trunk interface. The special bits are used in accordance with customer requirements. There are many possibilities to use the interface module as a user access point. Some examples are discussed below.

Framed; With or Without CRC

This is the basic way to connect pieces of equipment which use the G.704 frame structure to a DXX node. Only the data channels in time slots ts1…ts31 is transmitted over the network together with signalling data in the time slot ts16, if required.

The framing structure is demultiplexed at the interface point and only payload data will be supplied to the cross-connect system for further processing. In the transmitting direction the whole framing structure and the frame synchronization word are created in the interface and payload data from the cross-connect is added to the frame. The user equipment to be connected has usually no information about the protocol of the DXX system control channel. Therefore the HDLC channel will not be connected to the interface (with the exception of some DXX system modems). The free bits in time slot ts0 can be set to a state required by the user equipment. The synchronization remote end alarm indication bit RAI may be used, if required by the equipment to be connected. It is recommended to use the CRC check in the interface when the user equipment supports the use of CRC. Some equipment use the CRC E bits in a way not conforming to standards and in such cases unnecessary alarms can be avoided by setting the bits in a fixed state, usually 1.

When individual channel signalling is used, the multiframe structure in the receiving direction is demultiplexed in the interface and the signalling for each channel is transferred to the cross-connect for further processing. In the transmitting direction the multiframe synchronization time slot is created in the interface and stuffed with free bits. Signalling data from the cross-connect is placed into the signalling time slot. The free bits usually have the Permanent 1 state. If no signalling is used, then also time slot ts16 may be used to transmit payload data.

Framed; Transmission of Free Bits in ts0 Through the Network

It is possible to transmit the free bits of time slot ts0 through the DXX network when the equipment connected to a DXX node can utilize these free bits. Other functions may be the same as in the previous example. The free bits of time slot ts0, which are utilized by the application and transmitted through the network, are set to the X-conn state when the GDH (interface) module parameters are defined. The unit will then transmit these bits in the same state as it receives them from the cross-connect. Accordingly, bits received in time slot ts0 are supplied to the cross-connect in the same state as they are received.

On the transmission line the data transmission capacity is 4 kbit/s for one free bit in time slot ts0 due to the frame alternation. The total data transmission capacity of all five bits B4…B8 is thus 20 kbit/s. However, the DXX system utilizes a format where one free bit of time slot ts0 uses a capacity of 8 kbit/s on those connections on which it is transmitted through the network. Thus, a total capacity of 40 kbit/s is required to transmit all bits B4…B8 through the network. Transmission of the free bits of time slot ts0 always uses 64 kbit/s of the DXX node internal X-bus capacity for each interface, regardless of the number of transmitted bits.

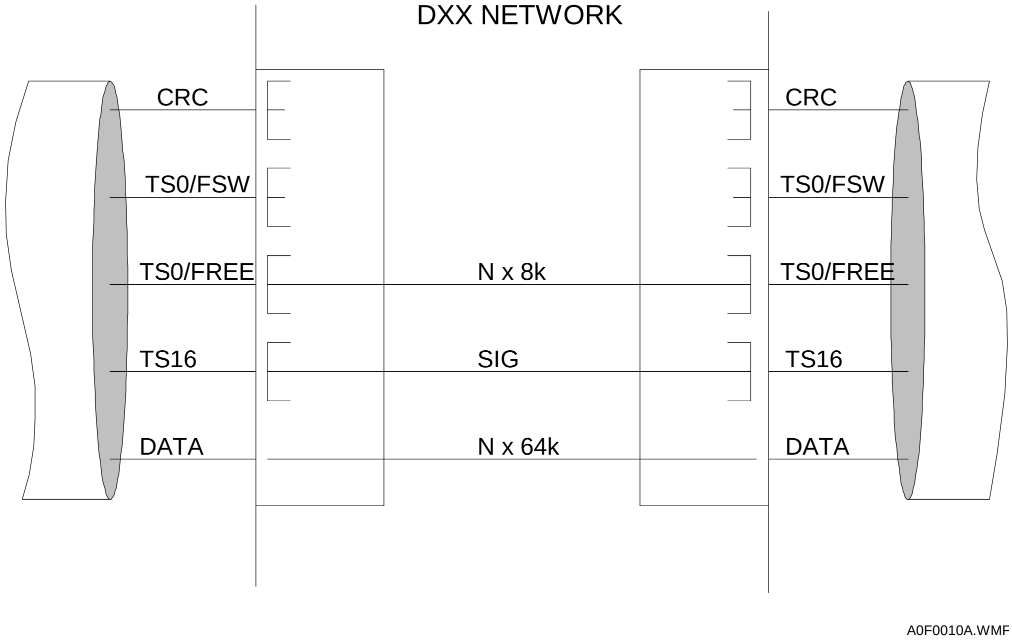

Fig. 20: TS0 Free Bits Connected Through the Network

Framed; Transmission of Time Slot ts0 Through the Network

It is possible to use the frame synchronization word to monitor the complete connection through the DXX network. In this case the whole time slot ts0 is directed via the cross-connect and transmitted to the far-end equipment. In this case the frame synchronization word, the free bits of time slot ts0 and the frame remote end alarm are transmitted over the whole connection. If it is required to connect signalling data separately over this connection, then the CRC check has to be regenerated in the user access interface. A new CRC check sum has to be calculated because the frame contents will change due to the different treatment of signalling data and normal data. The CRC check may be inactivated when the user equipment does not support the use of CRC.

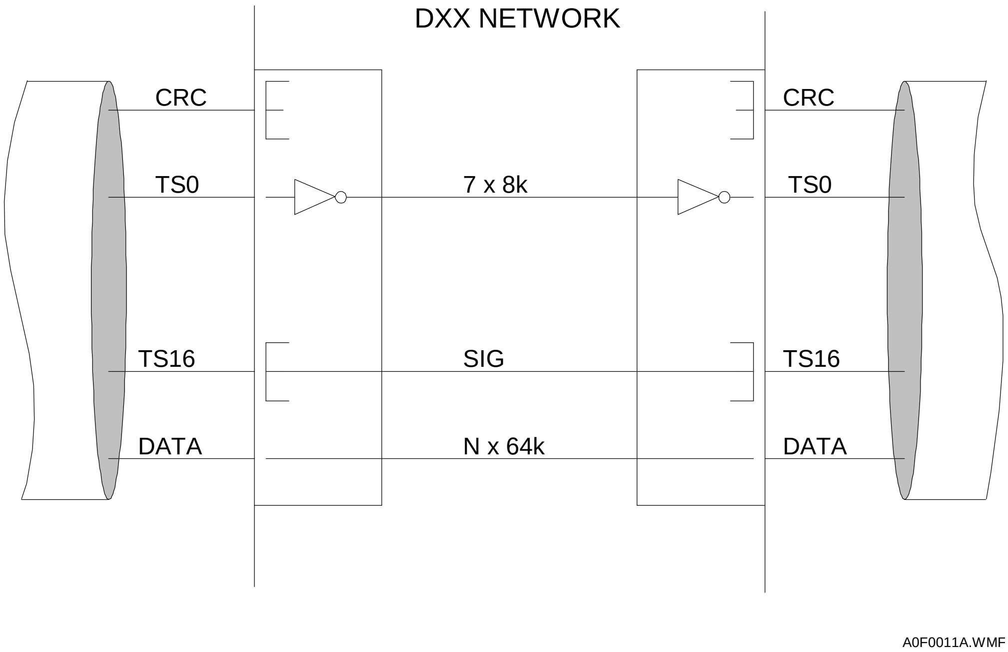

Fig. 21: TS0 Connected Through the Network

When it is connected to the transmission network, the time slot ts0 is inverted in the receiver before it is forwarded to the cross-connect. The time slot is in the inverted state when it is transmitted through the network, and in the far-end user access interface it is again inverted into its original format and then added to the frame as the synchronization time slot. The time slot ts0 is inverted so that it cannot cause false synchronization of the trunks when it propagates through the network. A trunk capacity of 56 kbit/s is used in order to transmit the whole time slot ts0 through the network. The transmission of the time slot ts0 uses 64 kbit/s of DXX node internal X-bus capacity for each interface.

When the interface parameters are set (during commissioning), the Fault consequence BER 10E-3 should be set Off. This causes received data with a bit error rate worse than 10E-3 (calculated with the aid of the frame synchronization word) to be connected through the network, and not to be set AIS as in normal transmission.

When the time slot ts0 is transmitted through the network, he user access interface will respond to errors in a way that is different from the normal. The remote end frame level alarm bit is not activated when the user access interface receiver detects a serious frame error, because this error will cause the remote end user equipment to respond, e.g. through the AIS, and to activate the remote end alarm bit. The remote end alarm bit is then transmitted back to the near-end user equipment. Moreover, the interface module will not respond to a received FrFEA bit. If an interruption occurs in the transmission network and an AIS is given instead of a payload signal to the interface, then this condition will be detected in the transmitter and an AIS is sent to the user equipment. The interface simultaneously activates the AIS from X-bus alarm.

Framed; Ts0 and CRC Connected Through the Network

It is possible to monitor the quality of the user's connection over the whole network with the aid of the CRC check. To enable this, a combination of the time slot ts0 and the CRC check is sent through the network from the near-end user equipment to the far-end user equipment. The CRC check sum is calculated for the total signal. In order to get equal results in the unit creating the CRC check sum and in the unit evaluating the CRC check sum, all bits must have the same state at both locations. The receiver will receive signalling data and payload data through different delays, and therefore it is not possible to use cross connected channel signalling, if the CRC check is transmitted over the connection. The idle data of possibly unused time slots has to be the same at both ends of the connection.

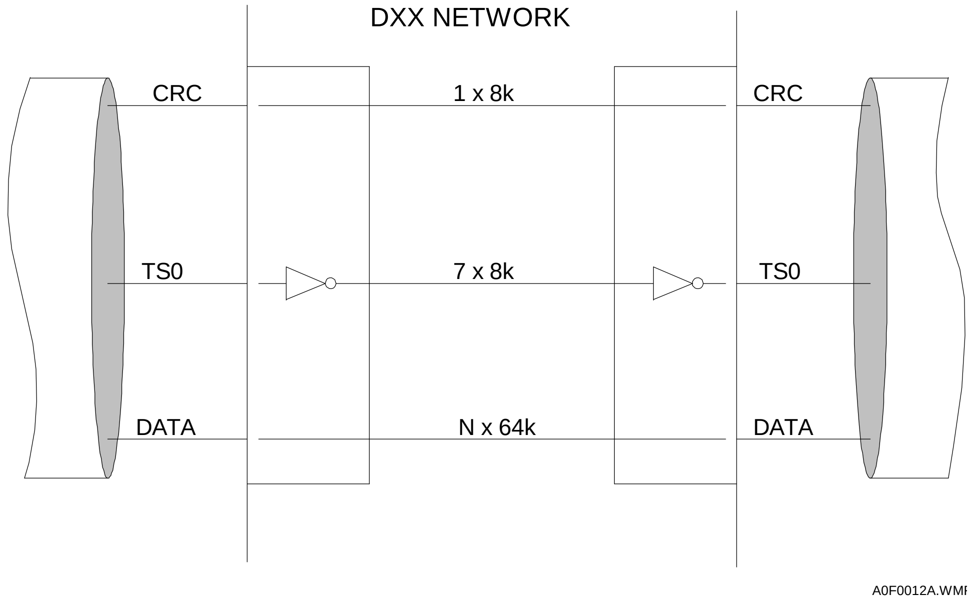

Fig. 22: TS0 and CRC Connected Through the Network

The time slot ts0 is inverted before it is transferred to the transmission network. A capacity of 64 kbit/s is used on a trunk line to transmit the combination of time slot ts0 and the CRC check, and 64 kbit/s of the internal DXX node cross-connect bus. CRC check E-bits indicating remote end block errors are also connected through the network. If these bits are not used they must set to the state 1. The interface responds to errors in the same way as when only time slot ts0 is connected through the network.

Transparent Without Frame

The interfaces of the module can also operate in a transparent mode. In this mode the received signal is connected through the network without any manipulations. The receiver is not synchronized to the incoming signal frame structure; no additions to the output signal are made in the transmitter. However, the receiver does cut the signal into slices of eight bits, which are transmitted through the network and from these slices a signal conforming to the original signal is then reconstructed in the receiver. In the transmission network a transparent signal requires a capacity according to its interface bit speed.

In order to use the interface in the transparent mode the interface parameter Framing must be set Off during parameterization. No frame errors are detected in the transparent mode, as the frames are not processed in any way. An alarm for error rate 10E-3 will be calculated only from code errors, whereas the error rate in a normal mode is calculated using also frame synchronization word errors.

Transparent With CRC Monitoring

The interface can be set to a function mode, in which the signal is transparently connected through the network, but in which the user access interface receiver synchronizes to the received signal frame structure and performs a CRC check on the signal. In the transmit direction the signal contents is not changed. The interface is set into this mode by defining the Framing parameter as CRC monitor during parameterization. The interface will also output framing error information, but actions on these errors are prevented.

1+1 Protection

Interfaces 1 and 2 can be 1+1 protected by each other. In protected mode both channels must have the same speed and framing mode settings. A unit working in the protected mode will look like a cross-connect port towards the X-bus. In the protected mode both channels transmit the same data signal coming from a buffer. Both channels use their own frame mux to create the frame structure. The receiving direction includes a change-over switch that selects the active receiver. Rx signal faults are classified into several categories. The switch uses fault categories to select the interface to be used. The fault categories are indicated in the fault table. For example 1.x means the first category (the worst or the most serious fault).

The operating modes of the change-over switch are:

- normal operation
- preferred operation
- forced operation

In the normal operating mode the switch will automatically switch to the other interface if the Rx signal fault category (1, 2, 3, 4, 5, OK) of the active interface continuously is worse than the fault category of the other interface, for a longer period than the given time delay. No switchover operation is activated when the categories are equal for both interfaces.

In the preferred operating mode a switch-over is triggered if there is a difference between the interface fault categories; the better interface is switched active. In a situation with equal fault categories for both interfaces the switch selects the preferred interface.

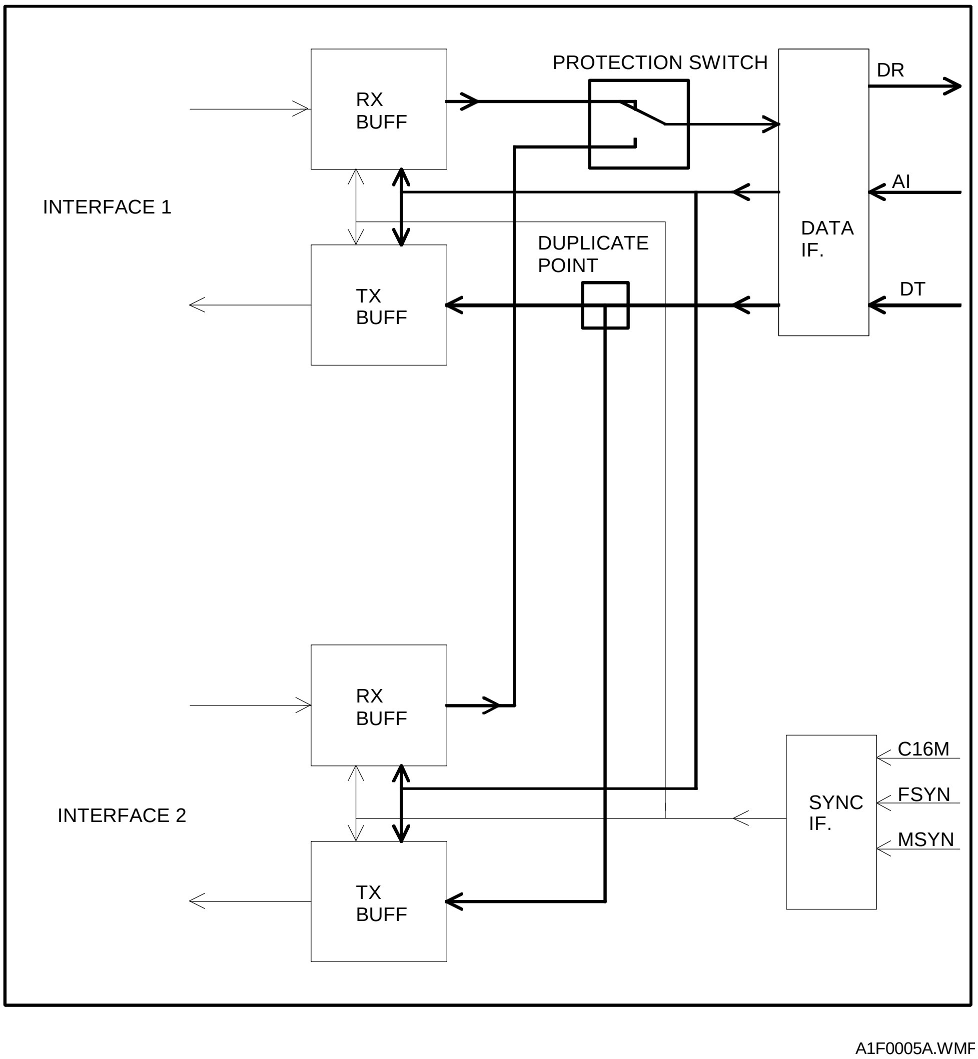

Fig. 23: Block Diagram of Protection

In forced operating mode the switch is forced to switch over without delay. Received data from the active interface is immediately connected to the X-bus. In this situation the Protection switch forced fault message with status MEI appears, and the red LED is turned on.

A switch operating time delay is defined for the prefer operating mode and the normal operating mode. The delay is defined as n x 10 ms, where n=0…6000; i.e. the delay is 0…1 minutes. The delay defines the allowed fault duration before the switch is triggered to switch over.

Fault and Service Status (PMA, DMA, MEI, S) in 1+1 Mode

In principle both interfaces generate their own alarms (alarm messages with fault status). PMA and S statuses are processed in this mode.

PMA Status Processing:

In the protection mode the normal PMA status is changed to the DMA status and there is an additional fault condition, Loss of protected signal, with a PMA status. In normal or preferred operating modes this special condition is created when both interfaces have a fault with fault category 3 or worse. In the forced operating mode this condition occurs if the forced interface has a fault with fault category 3 through 1. The inactive interface is not able to generate a fault with the PMA status.

S Status Processing:

In the protection mode an S status is generated only in the Loss of protected signal fault condition.

Far-End Alarms in 1+1 Mode

A far-end alarm indicates that the Rx signal is out of service (S status)

FrFEA	= Rx frame out of service
MFrFEA	= Rx multiframe out of service

Tx far-end alarms (FrFEA, MFrFEA) of both interfaces are generated assuming a fault status of the active interface. During a short period, when the change-over switch is in a transition phase, the far-end may generate an alarm even if there is no fault in the better interface. In forced operating mode only the active forced interface can cause far-end alarms to be sent.

RxAIS Processing

RxAIS and RxAIS to SigTS are always generated when FAE or MFrFAE is sent. AIS generating depends on the fault status of the selected interface.

Loops in G703-75/120-4CH interface module

The NMS is able to control several loops in the G703-75/120-4CH interface module. Loops and measurement points are used to find a faulty section of the line and to detect the faulty transmitting or receiving direction. The unit includes a loop time-out control which will turn off a loop when the user defined time has come to an end.

Interface Loop

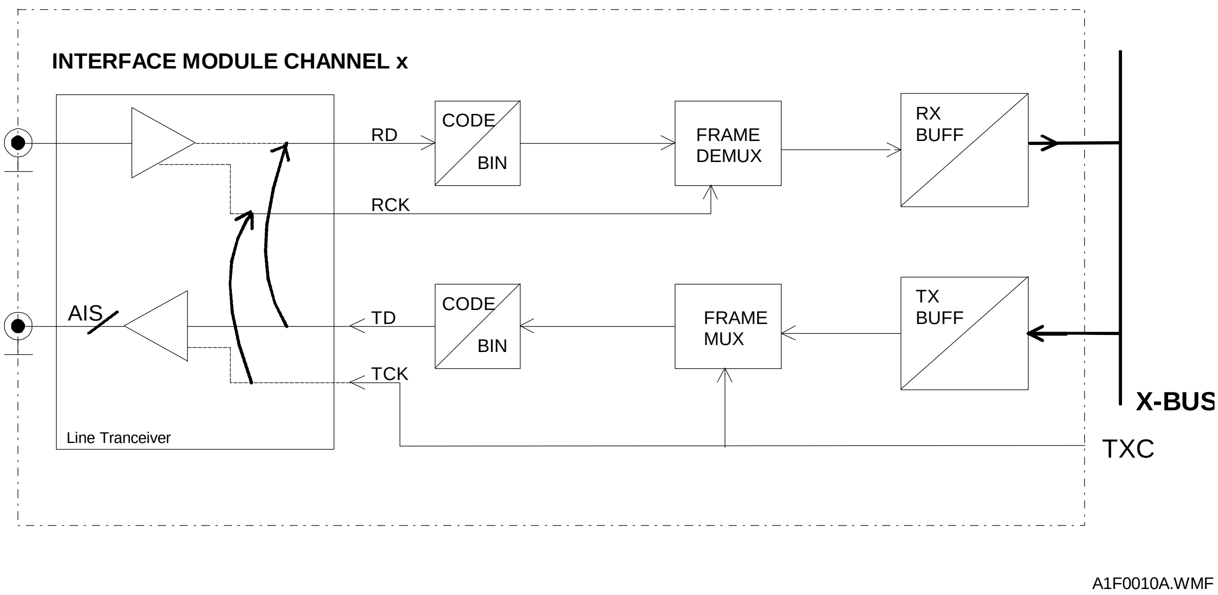

Fig. 24: Interface Loop

An interface loop is created in the interface tranceiver. It loops the transmit data and the clock signal back to the interface receiver. AIS is sent from the interface and the yellow alarm LED is switched on.

Equipment Loop

In an equipment loop the transmit data from the G.704 multiplexer before the line coder/decoder is looped back to the demultiplexer. The interface sends an AIS and the yellow alarm LED is switched on.

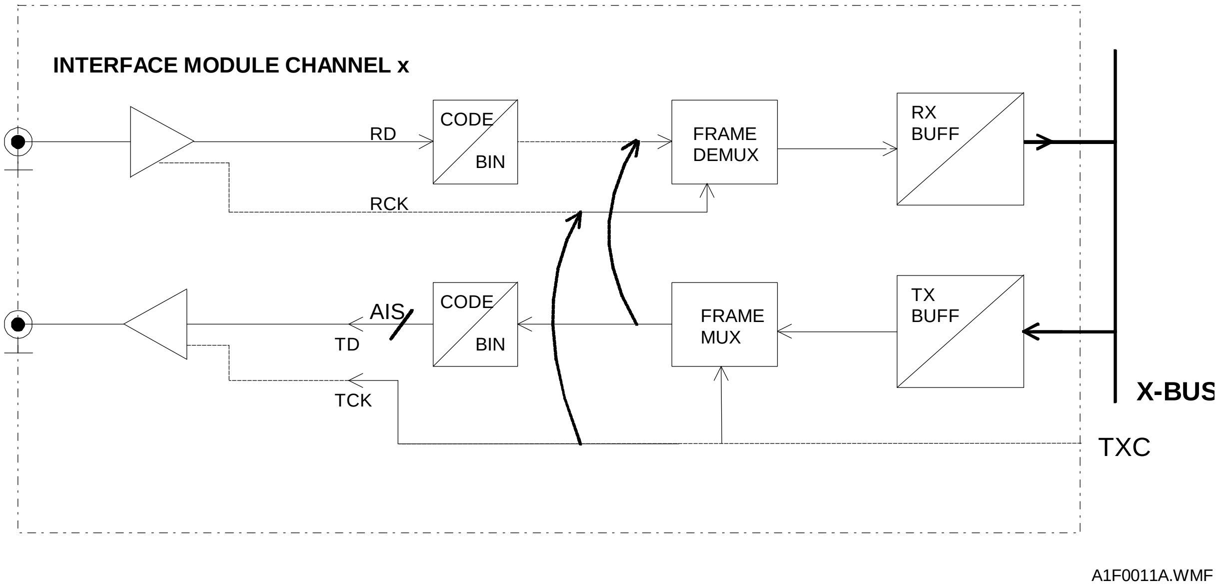

Fig. 25: Equipment Loop

This loop tests the frame multiplexer and demultiplexer. Neither the line coder/decoder nor the interface transceiver are included in the loop. It is also possible to detect faults in the transmitting and receiving buffers when a test signal from a measurement equipment is added to the signal passing through the looped channel. If no problems are detected with the interface loop, it is suggested to perform a test with the equipment loop to ensure that the module is in order.

Line Loop

In the line loop the Rx data received by the interface module is looped back to the interface transmitter. The received clock signal is used as the transmitter clock. AIS is connected to the X-bus instead of the received signal. The yellow alarm LED is switched on.

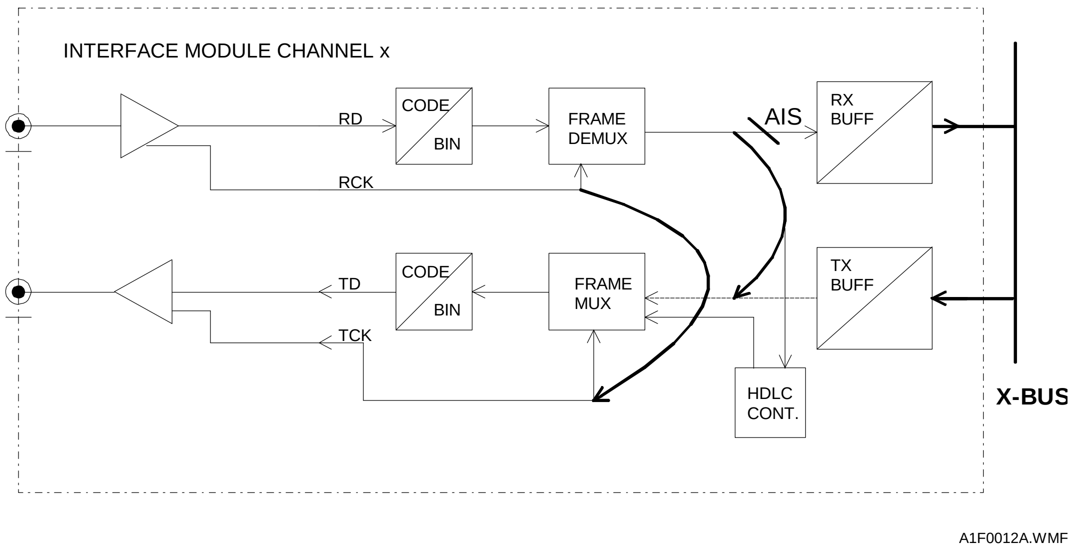

Fig. 26: Line Loop

The interface module, line coder and decoder as well as the frame demultiplexer and multiplexer can be tested from the module's line connector with the Line Loop Test. When it is used, the HDLC controller works with the line loop. All other bits are looped back to the interface.

Remote Line Loop

The remote line loop operates in the looped unit in the same way as the (local) line loop. The remote line loop is activated from the unit at the other end of the line. The loop is made via the HDLC channel and the control channel continues to operate even when the remote line loop is active. The status of the looped unit can be checked with the service computer. When the loop is made, the yellow LED of the unit which controls the loop is switched on, and the yellow LED of the looped unit is also switched on. The whole line can be tested with the remote line loop.

Clock RAI

The interface module can employ a dedicated bit of the frame structure as a far-end clock alarm bit. When a node loses the synchronization with the network, it activates the alarm bit. When the node receiving synchronization from the faulted node detects the alarm state of this bit, it can cease to use the corrupted clock and select the next clock source from the fallback list.

The NMS is able to select the bit used as a clock RAI. The user must choose a time slot and a bit for the clock RAI. The clock RAI time slot cannot be used for payload data. Special bits like HDLC can, however, be used in the same time slot with the clock RAI. The user must also select the polarity (active state).

The interface activates the clock RAI in the transmitting direction when it receives an alarm message from the cross-connect unit via the control bus. The clock RAI is inactivated in a corresponding manner.

In the Rx direction the clock RAI bit is separated from the incoming data and sampled by the processor with a sampling period of about 10 ms. The state of the bit is preserved when two consecutive equal states are detected. When a unit in the active state receives the clock RAI bit, it will cut off the SYB clock if it has one. If the cross-connect unit loses the SYB clock, it will select the next clock source in the fallback list. If the clock signal is lost for a short period, the interface module returns the clock to the SYB bus when the clock RAI is inactivated and then the cross-connect unit again will use the clock. If the synchronization is lost for a longer period, the cross-connect unit will remove the faulted interface from the SYB bus by a command through the control bus; thereafter the cross-connect unit directs a command to the next object in the fallback list without an SYB bus to have it connect the clock to the cleared SYB line.

G703-75/120-4CH Interface Module Front Panel

The module front panel houses two alarm LEDs, four channel interfaces and a synchronization interface which is of the same type as the channel interfaces. Service computer interface is located in XCG base unit.

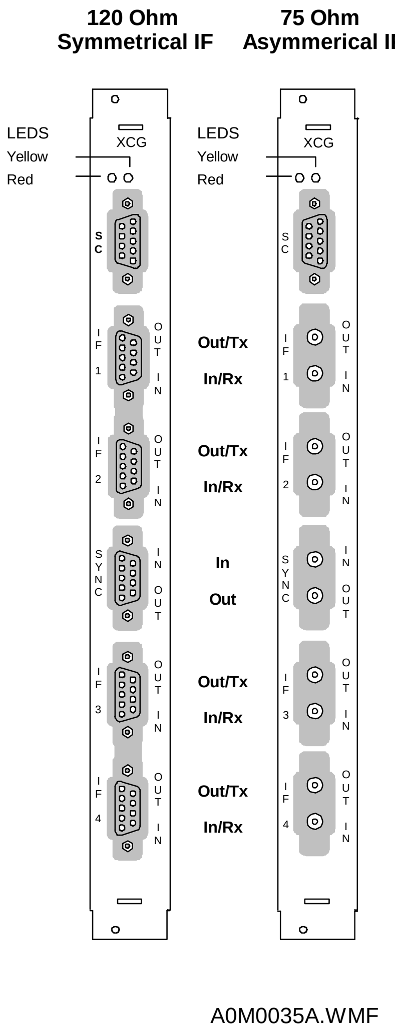

Fig. 27: G703-75/120-4CH modules installed in XCG base unit

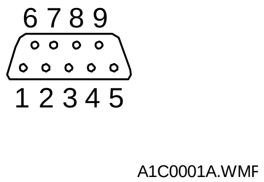

Fig. 28: 120 Ω balanced line interface (IF 1…4) connector pinout

Pin Usage for 120 Ω balanced line interface IF1-4 connector D9 Female

Pin	Signal
1	TxA
2	TxB
3, 6…9	GND
4	RxA
5	RxB

G703-75-4CH channel interface coaxial connector positions are shown Fig. 27.

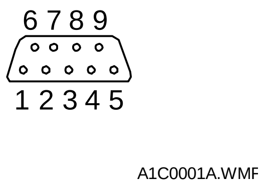

Fig. 29: 120 Ω balanced SYNC interface connector pinout

Pin Usage for 120 Ω balanced SYNC interface connector pinout D9 Female

Pin	Signal
1	Input A
2	Input B
3, 6…9	GND
4	Output A
5	Output B

G703-75-4CH SYNC interface coaxial connector positions are shown in Fig. 27.

G703-75/120-4CH Module Technical Specifications

Frame and Multiframe Operation

Filtering of FEA and MFrFEA bit:

The state of the alarm bit will switch if the opposite state is received three times consecutively.

AIS in frame 2048 kbit/s:

Signal containing two or less zeroes in a 2-frame period is recognized as an AIS signal. After AIS is detected, a signal containing three or more zeroes in a 2-frame period is recognized not to be an AIS signal.

AIS in multiframe:

A signal in the signalling time slots containing one or no zeroes in a multiframe period is recognized as an AIS signal.

Error rate 10E-3 limits from frame alignment word:

2048 kbit/s, Count time is four seconds	
Count to activate alarm:	94
Count to inactivate alarm:	17

Error rate 10E-3 limits from code errors:

2048 kbit/s, Count time is one second	
Count to activate alarm:	1973
Count to inactivate alarm:	229

CRC spurious frame alignment limits:

2048 kbit/s	915

Power requirement

GDH 522/521	3,5 W

Mechanics

Weight	grams
GDH 521	250
GDH 522	252

Module dimensions: 20 x 135 x 228 mm

Line Interfaces

Nominal impedance	75 Ω unbalanced/GDH 521	120 Ω unbalanced/GDH 522
Bit rate	2048 kbit/s ± 50 ppm	2048 kbit/s ± 50 ppm
Code	HDB3 (G.703 Annex A)	HDB3 (G.703 Annex A)
Pulse shape	G.703 figure 15	G.703 figure 15
Nominal peak voltage	2.37 V	3.0 V
Nominal pulse width	244 ± 25 ns	244 ± 25 ns
Attenuation margin	6 dB at 1024 kHz	6 dB at 1024 kHz
Input return loss	G.703 § 6.3.3	G.703 § 6.3.3
Output return loss	ETS 300 166 § 5.3	ETS 300 166 § 5.3
Jitter tolerance	G.823 § 3.1.1	G.823 § 3.1.1
Output jitter when transmit signal timing is supplied by the XCG operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)	< 0.05 UI (20 Hz…100 kHz)
Output jitter when the node is synchronized from any 2.048 Mbit/s G.703 interface or XCG external Clock input interface	TBR 12 § 5.2.1.4 TBR 13 § 5.2.1.4	TBR 12 § 5.2.1.4 TBR 13 § 5.2.1.4
Output short circuit current	< 50mA RMS (75Ω)	
Connector type	SMB	D-type 9-pin female connector
Overvoltage Protection	G.703 Annex B	G.703 Annex B

External Clock Input Interface (G.703 § 10.3)

Impedance	75Ω coaxial (GDH 521) or 120Ω symmetrical (GDH 522)
Nominal frequency	N x 64 kHz; N = 1…132
Frequency tolerance	± 50 ppm
Connector	SMB-connector male or 9-pin D-connector female
Input attenuation	6 dB at 2048 kHz max. relative to the output pulse
Return loss	15 dB min. at 2048 kHz
Over voltage protection	G.703 Annex B
Continuous signal level	5 V rms max.
Grounding	Cable shields are grounded

Node Clock Output Interface (G.703 § 10.2)

Impedance	75Ω coaxial (GDH 521) or 120 Ω symmetrical (GDH 522)
Connector	SMB-connector male or 9-pin D-connector female
Output pulse at 2048 kHz	see (G.703 § 10.2)
Pulse amplitude	V min = 0.75 V, V max. = 1.5 V at 75 Ω V min = 1.0 V, V max. = 1.9 V at 120 Ω
Nominal frequency	8448, 2048, 1408, 1024, 768, 704, 512, 384, 256, 192, 128, 64 kHz
Over voltage protection	G.703 Annex B
Grounding	Cable shields are grounded

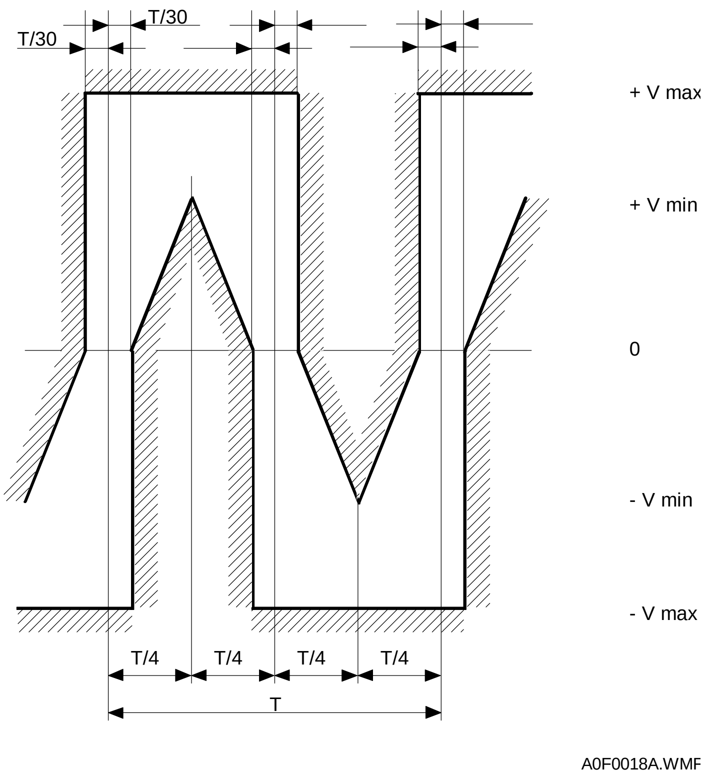

Fig. 30: Clock Output Pulse Mask at 2048 kHz

Jitter transfer function from 2 Mbit/s port A to 2 Mbit/s port B or from an external clock at 2048 kHz to a 2 Mbit/s port

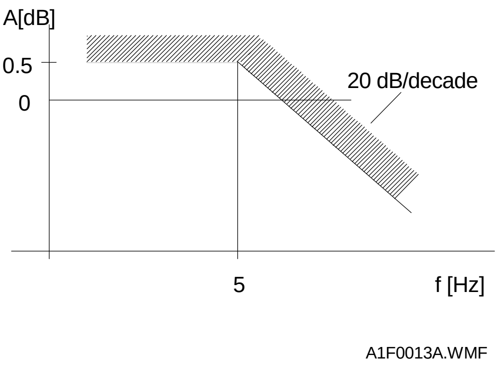

Fig. 31: Jitter Transfer Function

4.2.3.3 Faults and Actions

Terminology

The acronyms explained below will be used in the following tables:

PMA = Prompt Maintenance Alarm
DMA = Deferred Maintenance Alarm
MEI = Maintenance Event Information
S = Service Alarm
R = Red alarm LED
Y = Yellow alarm LED
RB = Red alarm LED blink
TxAIS = AIS insertion to Tx signal
RxAIS = AIS insertion to Rx signal
TxTS-AIS = AIS insertion in time slots of Tx signal
FrFEA = Frame level far-end alarm (ts0/B3 in 2Mbit/s frame)
MFrFEA = Multiframe level far-end alarm (FR0/ta sig/B6)
MFrFEA is also transmitted if FrFEA is transmitted.

XCG Faults

Fault Condition	Status	LED	Note
Reset of Unit	PMA	R	
Power Supply Faults			
Power + 5 V	PMA	R	
Power + 12 V	PMA	R	
Power - 10 V	PMA	R	
Memory Faults			
RAM Fault	PMA	R	
EPROM Fault	PMA	R	

Fault Condition	Status	LED	Note
Flash Write Error	PMA	R	
Flash Copy Error	PMA	R	
Flash Erase Error	PMA	R	
Flash Dublicate Error	PMA	R	
Flash Shadow Error	PMA	R	
Flash Check Sum Error	PMA, S	R	
Missing Settings	PMA	R	
Incompatible SW in EPROM and FLASH	PMA	R	
Cross-Connection Faults			
X-Connect RAM Fault	PMA, S	R	
Block 1/2/3/4 IA Fault	PMA, S	Y	
Loss of Master Clock Locking	MEI		
Fallback list Warning	MEI		
Loss of External Clock	PMA,	R	
Phase Locked Loop Alarm	PMA	R	
External Clock Warning	MEI		
Clock Far End Alarm of Choice 1/2/3/4/5	MEI	Y	
Flash List Check Sum Error	PMA, S	R	
ASIC Latch Error	PMA, S	R	
ASIC Latch Warning	MEI		
Time Controlled X-connect Warning	PMA		
X-Connect Flash List Conflict	MEI		
PortDesc Flash List Conflict	MEI		
Swapped Trunk Flash List Conflict	MEI		
Passivated Trunk Flash List Conflict	MEI		
Unit IA Fault	PMA, S	Y	
Inventory Faults			
Missing Unit	PMA, S	Y	Service alarm
Extra Unit	MEI	Y	

G703-75/120-4CH Interface Module Faults and Actions

Tx Signal Faults (Block 1, 2, 3, 4)

Fault Condition	Status	LED	Tx signal
Tx Clock fault (PLL)	PMA, S	R	TxAIS
Bus faults IA activity missing Bus sync. fault (block 0)	 PMA, S PMA, S	 R Y	 TxTS-AIS TxTS-AIS
AIS from X-bus	MEI, S	Y	TxAIS[a]

a Only when FAS is transferred through the network

Rx Signal Faults (Block 1, 2, 3, 4)

Signal & Frame Faults	**Status**	**LED**	**Rx signal**	**Tx signal**
1.1 Rx signal missing	PMA, S	R	RxAIS	FrFEA
1.2 Rx signal is AIS	MEI, S	Y	RxAIS	FrFEA
1.3 Loss of frame alignment 1.3.1 Frame alignment lost 1.3.3 Frame alignment lost by CRC -> 915/1000 errored CRC-blocks 1.3.2 CRC missing	 PMA, S PMA, S DMA	 R R R	 RxAIS RxAIS RxAIS	 FrFEA FrFEA FrFEA
1.4 BER 10-3 - frame alignment word (normal error response) - line code errors - n x 64 kbit/s baseband signal	PMA, S	R	RxAIS	FrFEA
1.5 Wrong input signal 1.5.1 Own NNM messages received 1.5.2 Wrong IDs in NNM messages (detection can be inhibited) 1.5.3 No response to NNM message	 PMA, S PMA, S PMA, S	 R R R	 RxAIS RxAIS RxAIS	 - - -
1.6 ASIC register error	PMA, S	R	-	-
Loops	Status	LED	Rx signal	Tx Signal
2.1 Local loops 2.1.1 Interface back to equipment 2.1.2 MUX/DEMUX back to eq. 2.1.3 MUX/DEMUX back to line 2.1.4 Line loop made by neighbour	 MEI, S MEI, S MEI, S MEI, S	 Y Y Y Y	 - - RxAIS RxAIS	 TxAIS TxAIS - -
2.2 Remote loops 2.2.1 Remote controlled line loop	 MEI, S	 Y	 -	 -
Multiframe level faults				
3.1 Multiframe alignment lost (group N)	PMA, S	R	RxAIS/ SigTS	MFrFEA
3.2 AIS in signalling (group N)	MEI, S	Y	RxAIS/ SigTS	MFrFEA
Far-end alarms	Status	LED	Rx signal	Note

Rx Signal Faults (Block 1, 2, 3, 4)

Signal & Frame Faults	**Status**	**LED**	**Rx signal**	**Tx signal**
4.1 Frame far-end alarm (FrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
4.2 Multiframe far-end alarm (MFrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
Degraded signal	Status	LED	RxAIS	FrFEA
5.1 Error rate 10-3 - frame alignment word (AIS insertion inhibited)	DMA	R	-	-
5.2 Error rate 10-6 - CRC block errors - line code errors	DMA	R	-	-
5.3 Frequency difference - excessive phase drift in input buffer	DMA	R	-	-
5.4 Buffer slips/1 hour	MEI	RB	-	-

Miscellaneous Faults (Block 1, 2)

Fault Condition	Status	LED	Rx signal	Tx signal
Port locking conflict	DMA	R	-	-
HDLC overlap with X-bus	DMA	R	-	-
Master clock RAI overlap with X-bus	DMA	R	-	-
G821 unavailable state	PMA, S	-	-	-
G821 limit event	DMA	-	-	-
Faults masked/Test	MEI	Y	-	-

1+1 Protection Switch Fault Messages (Block 0)

Fault Condition	Status	LED	Rx signal	Tx signal
Protection switch forced	MEI	R	-	-
Loss of protected signal	PMA, S	R	-[a]	-[a]

a Only when FAS is transferred through the network.

4.2.3.4 XCG Front Panel

Fig. 32 shows the connector locations and the LEDs. 75 Ω asymmetrical interface and 120 Ω symmetrical interface versions are available.

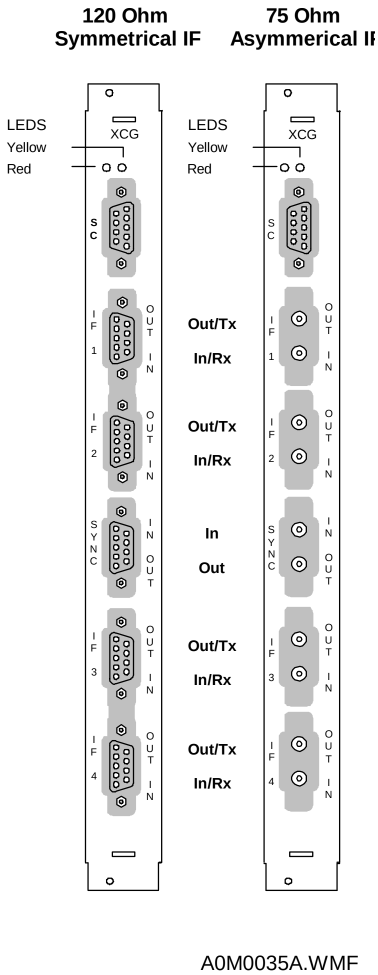

Fig. 32: G703-75/120-4CH interface modules installed in the XCG base unit

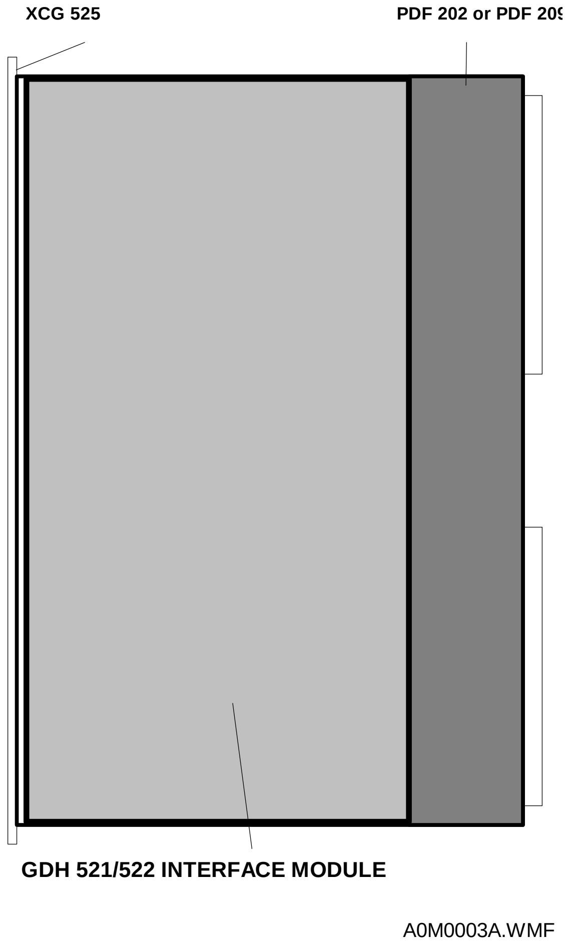

Fig. 33: XCG base unit

4.2.3.5 XCG Technical Specifications

Cross-Connect

Cross-connection method	**Synchronous time slot interleaving**
Frame frequency	8 kHz
Capacity: The sum of cross-connected signals	64 Mbit/s
Smallest cross-connect unit	8 kbit/s
Signalling cross-connection (XD)	n x 500 bit/s (CAS)
Delay of cross-connect core:	1 frame = 125 µs 2ms n x 64 kbit/s CAS-bits (500 bit/s)
Time integrity between time slots in cross-connected signals is maintained	
CAS TS capacity	= 32 bus time slots
n x 8 kbit/s cross-connect port capacity	= 95 bus time slots

Timing

Master clock frequency	16 896 kHz ± 30 ppm
Master clock functional modes	Locking to the IF rx clock (n x 64 kbit/s) n = 1 to 32
	Locking to external clock input (n x 64 kHz)
	Clock fallback list (5 levels + internal mode)
Frame sync.	8 kHz (125 us)
Multiframe sync (E1)	500 Hz (2ms)
Multiframe sync (T1)	166.66 Hz (6 ms)
Locking frequency	n x 64 kHz ±- 50 ppm
External clock input	n x 64 kHz (n = 1…32) ± 50 ppm
	Electrically G.703 (120 / 75 Ω)
External clock output	2048 kHz ± 30 ppm (Locked to master clock)
	Electrically G.703 (120 / 75 Ω)
Jitter transfer function and jitter in the output	G.736, G.823

The 16.896 Mhz clock is used to generate the main clock for whole node.

Control Interface Specifications

Service Computer Interface	
Purpose	Management interface for SC/NMS
Electrical interface	V.28
Data bit rate	9600 b/s asynchronous
Character format	8 bit, no parity, 1 stop bit
Connector type	D-type 9-pin female connector
Interface signals	102,103,104,105,106,107,108 and 109
Protocol	Layers 2…7 proprietary

Node Clock Jitter and Wander

Output jitter, measured within the frequency range 20 Hz to 100 kHz	
2 Mbit/s and clock port output, internal timing	0.05 UIp-p max.
2 Mbit/s port output, node synchronized from an external clock at 2048 kHz containing no jitter	0.05 UIp-p max.
2 Mbit/s port output, node synchronized from an interface at 2 Mbit/s containing no jitter	0.10 UIp-p max.

Input jitter tolerance at the external clock interface at 2048 kHz

See following figure.

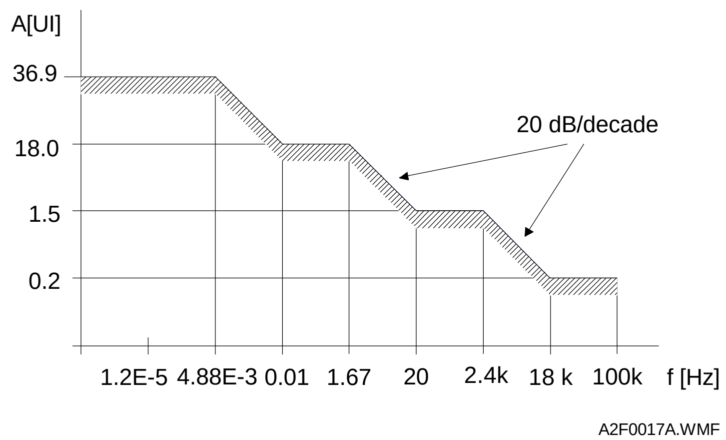

Fig. 34: Input Jitter Tolerance for the External Clock

Jitter transfer function from 2 Mbit/s port A to 2 Mbit/s port B or from an external clock at 2048 kHz to a 2 Mbit/s port

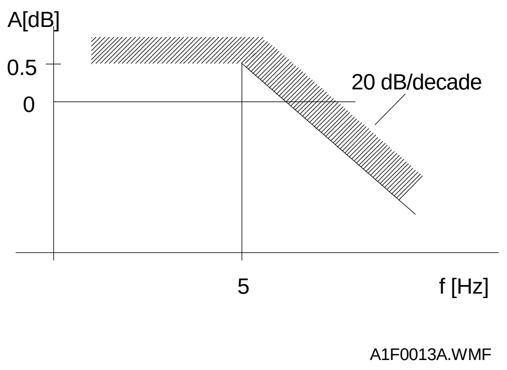

Fig. 35: Jitter Transfer Function

4.3 Installation and configuration

4.3.1 Midi Single Subrack (RXS-S8) in a 19" Rack

Assemble the numbered parts of Midi Single Subrack in the given order. The long mounting angle can be placed on either side. Part numbers in the instructions refer to (Midi Single Subrack).

Step 1. The subrack is installed in a 19" rack by using one short (#1) and one long (#2) mounting angle.

- Tighten the M5x10 size hex recessed head screws (#4) to the mounting angle (#1 or #2).
- If the hex recessed heads are too high and hinder installation, M5x10 size pan head screws can be used instead of the original screws.

Step 2. The cable channel (#11) included in the installation accessories is mounted to subrack using 2 M3x 10 DIN 965 screws.

Step 3. The air deflector plate (#10) is mounted to the rear of the subrack with two M3x8s (#9).

Step 4. The subrack is grounded with a separate grounding cable (#5) which is included in the subrack´s installation accessories. The cable is attached under the earthing nut (#7) of the subrack’s rear.

- A star washer (#6) must be inserted between the conductor lug terminal and the bottom panel to ensure electrical continuity between the subrack and the grounding conductor.

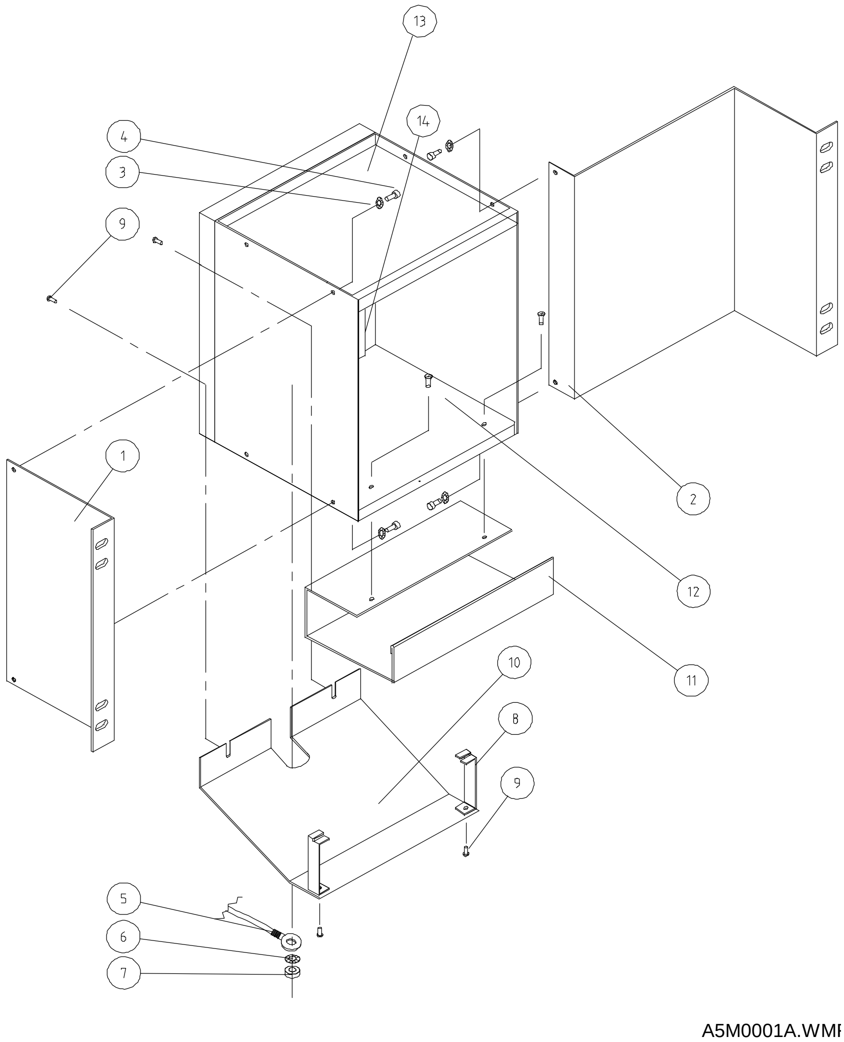

Fig. 36: Midi Single Subrack Assembly and Installation

Number	Title	Pcs.
1	Front mounting angle, short	1
2	Front mounting angle, long	1
3	Star washer, M5, DIN 6798A	4
4	M5x10, LK, HEX, DIN 912	4
5	Grounding cable 1.1m	1
6	Star washer, DIN 6798A	1
7	Nut, M6, DIN 934	1
8	Support rib	2
9	M3x8, LK, PZ, DIN 7985	4
10	Air deflector plate	1
11	Cable channel	1
12	M3x8, UK, PZ, DIN 965	2

4.3.2 Midi Double Subrack (two RXS-S8s) in a 19" Rack

A Midi Double Subrack is actually two RXS-S8s, Midi Single Subracks. Part numbers mentioned in the instructions below refer to next picture of Midi Double Subrack.

Step 1. Connect the Midi Single Subracks together with 4 M5x10 size hex recessed head screws (#3) and nuts (#1). Use a star washer (#2) under the screw.

Step 2. The Double Subrack is installed in a 19" rack by using two 105 x 26 x 2 mm size angle profiles for one shelf.

- Tighten the M5x10 size hex recessed head screws (#3) to the mounting angle (#4).
- If the hex recessed heads are too high and hinder installation, M5x10 size pan head screws can be used instead of the original screws.

Step 3. The cable channel (#11) included in the installation accessories is mounted to subrack using 2 M3x 10 DIN 965 screws (#12).

Step 4. The air deflector plate (#10) is mounted to the rear of the subrack with two M3x8s (#9).

Step 5. The subrack is grounded with a separate grounding cable (#5) which is included in the subrack´s installation accessories. The cable is attached under the earthing nut (#7) of the subrack’s rear.

- A star washer (#6) must be inserted between the conductor lug terminal and the bottom panel to ensure electrical continuity between the subrack and the grounding conductor.

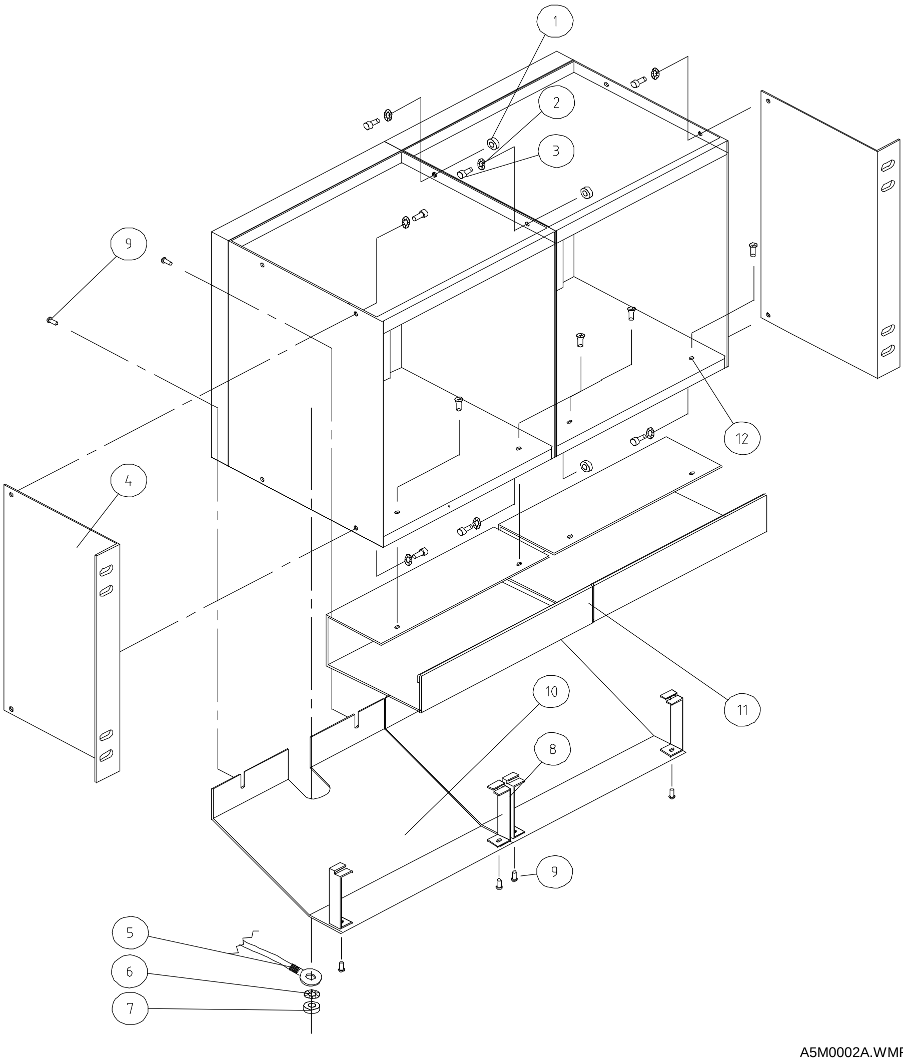

Fig. 37: Midi Double Subrack Assembly and Installation

Number	Title	Pcs.
1	Nut, M5, DIN 934	4
2	Star washer, M5, DIN 6798A	8
3	M5x10, LK, HEX, DIN 912	8
4	Front mounting angle, short	2
5	Grounding cable 1.1m	2
6	Star washer, DIN 6798A	2
7	Nut, M6, DIN 934	2
8	Support rib	4
9	M3x8, LK, PZ, DIN 7985	4
10	Air deflector plate	2
11	Cable channel	2
12	M3x8, UK, PZ, DIN 965	4

4.3.3 Table Top Installation Options

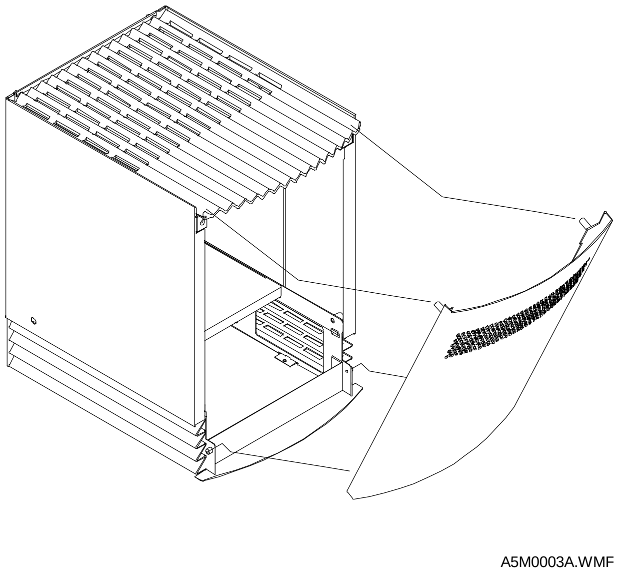

Fig. 38: How to remove Midi Node Front Cover

NOTE!

Hint: Place your fingers on the sides of the Midi Node and your thumbs on the upper edge of the front cover. Pull with your thumbs towards yourself. There are hinges on the bottom, but you can remove the door lifting it up.

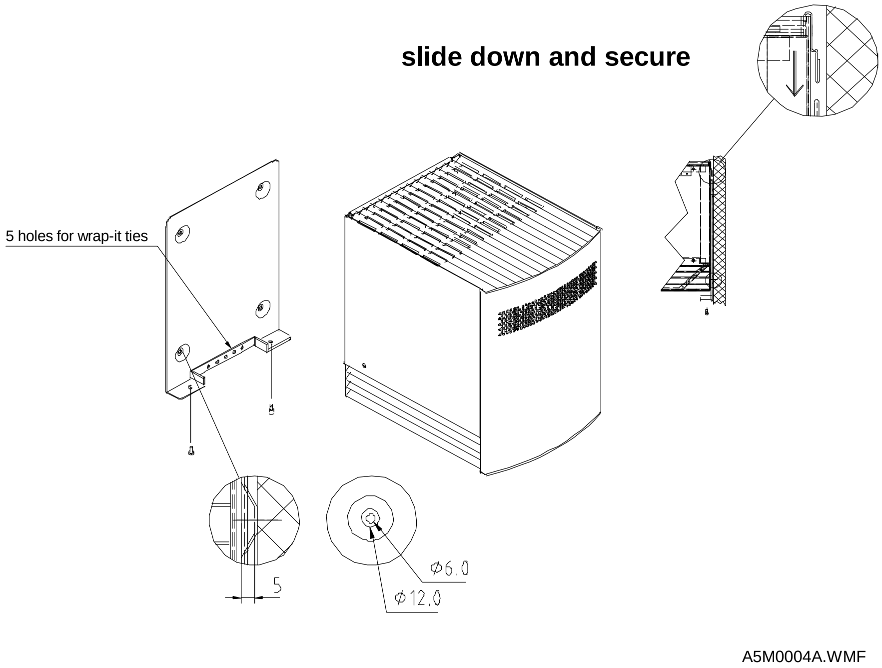

Fig. 39: Wall Installation

4.3.4 Requirements due to Extended Settings

AIU interface units have large configuration settings consuming extra non-volatile memory capacity extensively. This means some limitations to the installation of AIU units in Midi Nodes.

The XCG unit (with the software SMZ538 V2.0 or later) in a Midi Node provides the extended setting backup memory for

— 4 AIU 1:1 or

— 2 AIU 1:4 or

— 1 AIU 1:16.

The presence of AIU units does not limit the ability of an XCG unit to support the ordinary backup settings of typical DXX units.

4.3.5 Midi Node Configuration

4.3.5.1 Introduction

In this section the DXX node configuration is carried out using the following procedure:

Step 1. Select the node type: Midi Node.

Step 2. Select subrack type

Step 3. Select the cross-connect card type

Step 4. Select AC or DC power feed with or without redundancy.

Step 5. Select the interface units and interface modules based on the desired trunk and tributary interfaces.

Step 6. Check that you are not exceeding the limitations on mechanical space, cross-connect capacity, CAS cross-connect capacity or bit-level cross-connect capacity.

Step 7. Add cabinets to the inventory if required.

4.3.5.2 Configuration

Step 1. Select subrack type

- Every subrack has an XCG unit in slot 8.
- Thus the initial inventory is: Midi node: RXS-S8, XCG

Step 2. Select the cross-connect card type

- XCG takes care of the cross-connections, so a separate card is not needed.

Step 3. XCG cannot be protected.

Step 4. Select AC or DC power feed with or without redundancy.

- Since the Midi node inventory can vary a lot, it is very difficult to give instructions about the power consumption. Most of the time 80 W is more than enough. If optical interfaces or baseband modules are used, it is necessary to calculate the power consumption case by case. When rating fuses, please multiply the steady state consumption by 1…7 to allow for power up transients.
- The following options are available for power feed:
- Non-redundant DC feed. The following modules are required:
- Midi node: 1xPFU-A.
- Redundant DC feed. The following modules are required:
- Midi node: 1xPFU-A, 1xPFU-B.
- Non-redundant AC feed. The following modules are required:
- Midi node: 1xPAU-5T
- Redundant AC feed. The following modules are required:
- Midi node: 2xPAU-5T

Step 5. Select the interface units and interface modules based on the desired trunk and tributary interfaces.

- Midi Node supports the following trunk interfaces:

IF Use	IF Type	Module	Unit	IFs
8448/2048 kbit/s, G.704 frame	G.703	G703	GMH	1
2048 kbit/s, G.704 frame	G.703, 75Ω	G703-75	GMH	1
2048 kbit/s, G.704 frame	G.703, 120 Ω	G703-120	GMH	1
8448 kbit/s, G.704 frame	G.703, 75 Ω	G703-8M	GMH	1
8448/2048 kbit/s, G.704 frame	Optical LED	OTE-LED	GMH	1
8448/2048 kbit/s, G.704 frame	Optical laser	OTE-LP	GMH	1
n x 64 kbit/s (n = 2…6)	2/4W BB	BTE-384	GMH	1
320/576/1088 kbit/s	4W BB, 2B1Q	BTE-1088	GMH	1
1024/1088/2048/2112 kbit/s	4W BB, 2B1Q	BTE-2048	GMH	1
1088/2048 kbit/s	4W BB, HDB3	LTE	GMH	1
n x 64 kbit/s (n = 2…32)	V.35	V35-G704-BS	GMH	1
n x 64 kbit/s (n = 2…32)	V.36/V.11	V36-G704	GMH	1
n x 64 kbit/s (n=2…32)	X.21	X21-G704-S	GMH	1
n x 64 kbit/s (n=1…32)	V.35	V35-G704-BS	VMM	1
n x 64 kbit/s (n=1…32)	X.21	X21-G704-S	VMM	1
1544 kbit/s, T1 frame	T1, (G.703)	T1	GMM	2

— Midi Node supports the following tributary interfaces and user bit rates:

IF Use	IF Type	Module	Unit	IF
2048/8448 kbit/s, G.704 frame	G.703	G703	GMH	1
2048 kbit/s, G.704 frame	G.703, 75Ω	G703-75	GMH	1
2048 kbit/s, G.704 frame	G.703, 120Ω	G703-120	GMH	1
8448 kbit/s, G.704 frame	G.703, 75Ω	G703-8M	GMH	1
64A NTU 1.2 kbit/s…56 kbit/s	2/4W BB	BTE-64	GCH-A	1
64E NTU 2.4 kbit/s…64 kbit/s	2/4W BB	BTE-64	GCH-A	1
384A NTU n x 64 kbit/s (n = 1…5)	2/4W BB	BTE-384	GMH	1
384E NTU 38.4 kbit/s…384 kbit/s	2/4W BB	BTE-384	GCH-A	1
ISDN line card, 160kbit/s	2W BB		ISD-LN	4
STU-160 and ISDN NT1, 160kbit/s	2W BB		ISD-LT	4
STU-160 1.2 kbit/s…128 kbit/s	2W BB		IUM-5T or IUM-10T	4 or 8
STU-1088 n x 64 kbit/s (n = 1…16)	4W BB	BTE-1088	GMH	1
STU-2048 n x 64 kbit/s (n = 1…32)	4W BB	BTE-2048	GMH	1
2048 kbit/s transparent	G.703	G703	GCH-A	1
600 bit/s…2048 kbit/s sync. 0 bit/s…64 kbit/s async.	V.35	V35	VCM-10T-A	2
600 bit/s…2048 kbit/s sync. 0 bit/s…64 kbit/s async.	V.36/V.11	V36	VCM-10T-A	2
600 bit/s…2048 kbit/s sync. 0 bit/s…64 kbit/s async. (D25 connector)	V.35	V35-IEC	VCM-5T-A	2
600 bit/s…2048 kbit/s sync. 0 bit/s…64 kbit/s async. (D25 connector)	V.36/V.11	V36-IEC	VCM-5T-A	2
600 bit/s…2048 kbit/s sync.	X.21	X21	VCM-5T-A	2
600 bit/s…64 kbit/s sync. 0 bit/s…64 kbit/s async.	V.24/V.28	V24-DCE	VCM-5T-A	2
600 bit/s…64 kbit/s sync. 0 bit/s…64 kbit/s async.	V.24/V.28 (DTE)	V24-DTE	VCM-5T-A	2
64 kbit/s co/contra	G.703	G703-64	VCM-5T-A	2
VF with 64 kbit/s PCM. (E & M with the module EM-2x10)	2/4W, G.712/ G.713	PCM-10VF (EM-2x10)	CAE	10
VF with 64 kbit/s PCM and 32/24/16 kbit/s ADPCM. (E & M with the module EM-2x10)	2/4W, G.712/ G.713	ADPCM-10VF (EM-2x10)	CAE	10
1544 kbit/s, T1 frame	T1	T1	GMM	2
POTS Central Office (exchange, PA-BX) side 64 kbit/s PCM, country dependent	2W, G711	CCO	CAE	10
POTS Central Office (exchange, PA-BX) side ADPCM 32, 16kbit/s, country dependent	2W, G711	CCO-ADPCM	CAE	10

IF Use	IF Type	Module	Unit	IF
POTS subscriber side, 64 kbit/s PCM,. country dependent	2W, G711	CCS	CAE	10
POTS subscriber side, 64 kbit/s PCM, country dependent	2W, G711	CCS-ADPCM	CAE	10

— The Midi Node also supports server cards. EAE is a PCM/ADPCM compression card. Each EAE supports 30 PCM/ADPCM conversions. VCM-xT-A and GCH-A units can be used as point-to-multipoint servers. EPS-5T/EPS-10T is a voice/fax compression unit. ECS-xT is used in Midi Node to convert X.50 signals to V.110 or vice versa.

Step 6. Check that you are not exceeding the limitations on mechanical space, cross-connect capacity, CAS cross-connect capacity or bit level cross-connect capacity.

— The following units require one slot: PAU-5T, GMH, VCM-5T-A, GCH-A, EAE, EPS-5T, VMM, GMM, and XCG. The following units take two slots: VCM-10T-A, CAE, and EPS-10T.

— The cross-connect capacity of is 1043 X-bus time slots. If you exceed this limit, you have to move interfaces to other nodes or you have to decrease the bit rate of some interfaces.

— Different units use different methods for allocating capacity from the X-bus. VCM-xT-A, GCH-A and CAE allocate capacity when the interfaces are first configured. The required X-bus capacity is the XB-capacity rounded up to the next full time slot. Since the cross-connect granularity of a basic node is 8 kbit/s, XB-rate has to be an integer multiple of 8 kbit/s. Sub-rates of 64 kbit/s are mapped into n x 8kbit/s using V.110 mapping. V.110 maps the user rates to the following XB-rates:

User rate	XB rate
600 bit/s	8 kbit/s
1200 bit/s	8 kbit/s
2400 bit/s	8 kbit/s
4800 bit/s	8 kbit/s
7200 bit/s	16 kbit/s
9600 bit/s	16 kbit/s
12000 bit/s	32 kbit/s
14400 bit/s	32 kbit/s
19200 bit/s	32 kbit/s
38400 bit/s	64 kbit/s
48000 bit/s	64 kbit/s
56000 bit/s	64 kbit/s

— At these V.110 rates end-to-end CRC, transfer of control signals through the network and network independent clocking are supported without any extra overhead. At n x 64 kbit/s user rates these special functions require an additional m x 8 kbit/s frame. Depending on the desired functionality and on the user bit rate, the capacity of the additional frame is shown in the following table:

105/109 Transfer	CRC	Network Independent Clocking	User Rate < = 512 kbit/s Frame Rate kbit/s	User Rate > 512 kbit/s Frame Rate kbit/s
ON			8	8
	ON		8	8
		ON	8	24
ON	ON		16	16
ON		ON	16	24
ON	ON	ON	16	24
	ON	ON	8	24

— For example, if a V.35 interface is used at 512 kbit/s without any special features the XB-capacity is 8 x 64 kbit/s or 8 time slots and the required X-bus capacity is also 8 bus time slots. If the same 512 kbit/s circuit is created with end-to-end CRC supervision, the XB capacity is 520 kbit/s or 8 time slots and 1 bit. The required X-bus capacity is 9 bus time slots.

— If GMH is used in unframed mode, it works like VCM-xT-A, GCH-A and CAE. For 2048 kbit/s and 8448 kbit/s G.704 framed interfaces the cross-connect capacity allocation method depends on the receive buffer length of the interface. The buffer length can be either short (2 frames) or long (4/8/64 frames). Short buffer enables even allocation of XB-capacity, which means that the whole capacity is allocated when a port is first configured. Long buffer enables uneven allocation of XB-capacity, which means that only the CAS time slots are allocated when the interface is first configured and the rest of the capacity is allocated as cross-connections are made. Using uneven allocation, it is possible to equip a node with more than 32 x 2048 kbit/s ports, if the number of connected time slots plus CAS time slots is less than or equal to 1043.

— Different GMH and GMM interface types allocate X-bus capacity using the following methods:

IF type	Allocation	X-Bus Time Slots
8448 kbit/s, G.704 framed	Even	130
2048 kbit/s, G.704 framed	Even	32
8448 kbit/s, G.704 framed	Uneven	0/1/2/3/4 + connected time slots
2048 kbit/s, G.704 framed	Uneven	0/1 + connected time slots
n x 64 kbit/s, framed	Uneven	0/1 + connected time slots
2048 kbit/s transparent	Uneven/even	32
n x 64 kbit/s, unframed	Uneven	n
1544 kbit/s, T1 framed	Even	32
1544 kbit/s, T1 framed	Uneven	0/1 + connected time slots
1544 kbit/s, transparent	Uneven	25

— The CAS capacity of XCG is 32 time slots. CAS can be independently enabled or disabled in each interface. The interfaces require the following amounts of CAS time slots depending on whether CAS is enabled or disabled:

IF Type	Allocation	CAS TS, XCG
8448 kbit/s, G.704 framed	Even	0/1/2/3/4
2048 kbit/s, G.704 framed	Even	0/1
8448 kbit/s, G.704 framed	Uneven	0/1/2/3/4
2048 kbit/s, G.704 framed	Uneven	0/1
n x 64 kbit/s, framed	Uneven	0/1
CAE unit with E&M	Uneven	1
1544 kbit/s, T1 framed	Even	0/1
1544 kbit/s, T1 framed	Uneven	0/1

Step 7. Add cabinets to the inventory if required.

— For compliance with EN 55022 Class A you can use CAB-2D cabinets. In this case the customer can also use some other cabinet types.

— For compliance with EN 55022 Class B, you must use the EMCC-S/D/2D cabinets or RXS-S8-TT if used in tabletop solutions. Other cabinet types cannot be used.

4.3.5.3 Midi Node Configuration Example

This example covers the configuration of a Midi Node with the following interfaces:

— 2 x 8448 kbit/s G.703/G.704 trunk interfaces

— 2 x 2048 kbit/s G.703/G.704 trunk interfaces

— 2 x n x 64 kbit/s G.703/G.704 tributary interfaces

— 2 x NTU interfaces with user bit rate of 19.2 kbit/s (STU-160)

— 2 x NTU interfaces with user bit rate of 704 kbit/s (STU-1088)

— 2 x n x 64 kbit/s V.35 interface

— 2 x n x 64 kbit/s V.36/V.11 interface

— 2 x 9600 bit/s V.24/V.28 interface

Non-redundant AC power feed is used. CAS will be active in all framed interfaces.

Step 1. Select subrack type

— We select RXS-S8.

— The initial inventory is: RXS-S8, XCG.

Step 2. Select the cross-connect card type

— XCG takes care of the cross-connections

Step 3. Select AC or DC power feed with or without redundancy

— We select non-redundant AC feed.

— The total inventory will be:

— RXS-S8, XCG, PAU-5T.

Step 4. Select the interface units and interface modules based on the desired trunk and tributary interfaces.

The following modules are required:

Interface	**Modules**
2 x 8448 kbit/s G.703/G.704 trunk interfaces	GMH, 2 x G703
2 x NTU interfaces with user bit rate of 19.2 kbit/s (STU-160)	IUM-5T
2 x NTU interfaces with user bit rate of 704 kbit/s (STU-1088)	GMH, 2 x BTE-1088
2 x n x 64 kbit/s V.35 interface	½ xVCM-10T-A, V35
2 x n x 64 kbit/s V.36/V.11 interface	½xVCM-10T-A, V36
2 x 9600 bit/s V.24/V.28 interface	½xVCM-5T-A, V24-DCE

Step 5. Check that you are not exceeding the limitations on mechanical space, cross-connect capacity, CAS cross-connect capacity or bit level cross-connect capacity.

The following units are included in the total inventory:

— PAU-5T, 2 x GMH, IUM-5T, VCM-10T, VCM-5T, XCG.

— Since the maximum bit rate of n x 64 kbit/s interfaces has not been specified, we will assume 2048 kbit/s to be on the safe side.

Interface	**X-bus Ts**
2 x 8448 kbit/s G.703/G.704 trunk interfaces	2 x 130
2 x 2048 kbit/s G.703/G.704 trunk interfaces in XCG	2 x 32
2 x n x 64 kbit/s G.703/G.704 tributary interfaces in XCG	2 x 32
2 x NTU interfaces with user bit rate of 19.2 kbit/s (STU-160)	2 x 1
2 x NTU interfaces with user bit rate of 704 kbit/s (STU-1088)	2 x 11
2 x n x 64 kbit/s V.35 interface	2 x 32
2 x n x 64 kbit/s V.36/V.11 interface	2 x 32
2 x 9600 bit/s V.24/V.28 interface	2 x 1
Total	542

The CAS capacity usage is

Interface	**CAS Ts**
2 x 8448 kbit/s G.703/G.704 trunk interfaces	16
2 x 2048 kbit/s G.703/G.704 trunk interfaces	4
2 x n x 64 kbit/s G.703/G.704 tributary interfaces	4
Total	24

Step 6. Add cabinets to the inventory if required.

The total inventory of this example will be:

Unit	Description	Quantity
BTE-1088	1088 kbit/s baseband interface module for GMH. 1 IF.	2
IUM-5T	STU-160 interface unit. 4 IF.	1
RXS-S8-TT	Midi table top case	1
G703-75	2048/8448 kbit/s G.703 interface module. 1 interface	2
G703-75-4CH	2048 kbit/s G.703 interface module for XCG 4 IF	1
GMH	G.704 Framed interface unit. 2 interfaces / unit.	2
PAU-5T	AC power supply	2
RXS-S8	Midi subrack	1
XCG	System control/Cross-connect unit	1
V24-DCE	V.24/V.28 interface module for VCM-5T-A. 2 IFs.	1
V35	V.35 interface module for VCM-10T-A. 2 Interfaces	1
V36	V.36/V.11 interface module for VCM-10T-A. 2 IFs	1
VCM-5T-A	Unframed data interface unit. 4 interfaces / unit	1
VCM-10T-A	Unframed data interface unit. 4 interfaces / unit	1

4.4 Technical Specifications

All CCITT references concern the Blue Book, 1988. When applicable, the references to former CCITT Recommendations have been amended to ITU-T references. These references include the date of the valid ITU-T Recommendation in case these are revised in the future. If a CCITT Recommendation has not been updated as ITU-T by the International Telecommunication Union, CCITT is used in this document.

4.4.1 Relevant Recommendations

The ITU-T/CCITT recommendations concerning DXX trunk interfaces and user access points are:

Rec.	ITU-T Date (CCITT 1988)	Main Characteristics of the Node and Trunk Interfaces
G.651	March 1993	Characteristics of a 50/125
G.652	March 1993	Characteristics of a single-mode optical fibre cable
G.703	April 1991	Physical/electrical characteristics of hierarchical digital interfaces
G.704	CCITT	Synchronous frame structure used at primary and secondary hierarchical levels
G.706	CCITT	Frame alignment and CRC procedures for G.704 frames
G.707	October 1995	Network node interface for the SDH
G.726	December 1990	40, 32, 24, 16 kbit/s adaptive differential pulse code modulation (ADPCM)
G.732	CCITT	Characteristics of a primary PCM multiplexing equipment operating at 2048 kbit/s
G.736	March 1993	Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s
G.744	CCITT	Second order PCM multiplex equipment operating at 8448 kbit/s
G.761	CCITT	General characteristics of a 60-channel transcoder equipment
G.775	November 1994	Loss of signal (LOS) and Alarm Indication Signal (AIS) defect detection and clearance criteria
G.781	January 1994	Structure of recommendations for SDH
G.782	January 1994	Types and general characteristics of SDH equipment
G.783	January 1994	Characteristics of SDH equipment functional blocks
G.803	March 1993	Architectures of transport networks based on the SDH
G.811	CCITT	Timing requirements at the outputs of primary reference clocks suitable for plesichronous operation of international digital links
G.81s (813)	July 1995	Timing requirements at the outputs of slave clocks suitable for SDH operation on international digital links
G.821	CCITT	Error performance of an international digital connection
G.823	March 1993	Control of jitter and wander on the 2048 kbit/s hierarchy
G.825	March 1993	The control of jitter and wander within digital networks which are based on the SDH hierarchy
G.826	November 1993	Error performance parameters and objectives for international constant bit rate digital paths at or above the primary rate
G.832	November 1994	Transport of SDH elements on PDH networks
G.841	May 1995	Types and characteristics of SDH protection architectures
G.957	July 1995	Optical interfaces for equipments and systems relating to the synchronous digital hierarchy
G.960	March 1993	Digital transmission system on metallic local lines for ISDN basic rate access

The ITU-T/CCITT recommendations concerning DXX trunk interfaces and user access points are:

Rec.	ITU-T Date (CCITT 1988)	Main Characteristics of the Node and Trunk Interfaces
G.961	March 1993	Access digital section for ISDN primary rate at 2048 kbit/s
Q.921	March 1993	ISDN user-network interface – Data link layer specification

Standard Transmission Network Interfaces (2 Mbit/s and 8 Mbit/s)

2048 kbit/s framed interface	G.704, G.706, G.732, G.736, G.821, G.823
8448 kbit/s framed interface	G.704, G.744, G.821, G.823

User Access Points For Unframed Data Interfaces

Recommendation[a]	Description
V.11 (ITU-T 03/93)	Electrical characteristics for balanced double-current interface circuits
V.13 (ITU-T 03/93)	Simulated carrier control
V.14	Transmission of start-stop characters over synchronous bearer channels
V.22	1200 bits per second duplex modem standardized for use in the general switched telephone network and on point-to-point 2-wire leased telephone-type circuits
V.24	Interface circuits between DCE and DTE
V.27 ter (CCITT 10/84)	4800/2400 bits per second modem standardized for use in the general switched telephone network
V.28	Electrical characteristics for unbalanced double-current interchange circuits
V.29	9600 bits per second modem standardized for use on point-to-point 4-wire leased telephone-type circuits
V.32	A family of 2-wire, duplex modems operating at data signalling rates of up to 9600 bit/s for use on the general switched telephone network and on leased telephone-type circuits
V.35 (CCITT Red Book)	Data transmission at 48 kbit/s using group band modem
V.36	Modems for synchronous data transmission using group band modems
V.54	Loop test devices for modems
V.110 (ITU-T 09/92)	ISDN rate adaption for V-series interfaces
X.21 (ITU-T 09/92)	Synchronous data network interface between DCE and DTE
X.25 (ITU-T 03/93)	Interface between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE) for terminals operating in the packet mode and connected to public data networks by dedicated circuit
X.27	Same as V.11
X.30	ISDN rate adaption for X.21 interfaces
X.50	Fundamental parameters of a multiplexing scheme for the international interface between synchronous data networks.
X.50bis	Fundamental parameters of a 48-kbit/s user data signalling scheme for the international interface between synchronous data networks.
X.54	Allocation of channels on international multiplex links at 64 kbit/s.

a All recommendations CCITT except those listed as ITU-T

User Access Points for Voice Frequency Interfaces

G.711 (CCITT)	64 kbit/s PCM encoding
G.712 (CCITT)	4-wire voice frequency interface
G.713 (CCITT)	2-wire voice frequency interface
G.721 (CCITT 1986/88)	32 kbit/s ADPCM

4.4.2 Relevant SDH Standards

ETSI Standards

ETS 300 147	SDH multiplexing structure, Jan 1995
ETS 300 417-1-1	Generic functional requirements for SDH transmission equipment
	Generic processes and performance, Feb. 1995
DE/TM-1015	Generic functional requirements for SDH transmission equipment
	part 2 Physical section layer functions, March 95
	part 3 STM-N regenerator and multiplex section layer functions, May 95
	part 4 SDH path layer functions, June 95
	part 6 Synchronisation distribution layer functions, June 95
DE/TM-3017	Generic requirements for synchronous networks
	Part 1 Definitions of synchronisation terminology, Oct. 94
	Part 2 Synchronisation network architecture, Mar 95
	Part 3 The control of jitter and wander within synchronisation networks, Sep. 95
	Part 5 Timing characteristics of slave clocks suitable for operation in SDH eq., May 95
DE/TM-3042	SDH Network Protection Schemes: APS Protocols and operation, Aug. 95

ETSI Technical Reports

DTR/TM-3025 SDH Network Protection Schemes: Types and characteristics, Sep. 95

T1 Recommendations

- Bellcore TR-TWT-000170 Digital Cross-Connect System (DCS 1/0) Generic Requirements and Objectives; 1993
- ANSI T1.403 - 1989 Carrier to Customer Installation - DS1 Metallic Interface
- TR 54016 - 1989 Requirement for interfacing Digital Terminal Equipment to Services employing the Extended Superframe Format
- ACCUNET T1.5 Service - Description and Interface Specification - 1989 (AT&T)
- FCC-68 Connection of terminal equipment to the telephone network
- ITU Recommendations G.802 Interworking between networks based on different digital hierarchies ans speech encoding laws
- Bellcore TA-TSY-000499 Transport Systems Generic Requirements (TSGR):Common Requirements
- Bellcore TA-TSY-000342 High Capacity Digital AccessService, Transmission Parameter Limits and Interface Combinations - Issue 1 -1990
- TR-NWT-000820 - 1993 Network Maintenance:Transport Surveillance - Generic Digital Transmission Monitoring

4.4.3 Relevant ATM standards

ITU-T recommendations

I.150	B-ISDN Asynchronous Transfer Mode Functional Characteristics	ITU-T 11/95
I.311	B-ISDN General Network Aspects	ITU-T 08/96
I.321	B-ISDN Protocol Reference Model and Its Application	ITU-T 1991
I.326	Functional Architecture of Transport Networks Based on ATM	ITU-T 11/95
I.327	B-ISDN Functional Architecture	ITU-T 03/93
I.356	B-ISDN ATM Layer Cell Transfer Performance	ITU-T draft 6R/1996
I.361	B-ISDN ATM Layer Specification	ITU-T 11/95
I.371	Traffic Control and Congestion Control in B-ISDN	ITU-T 08/96
I.413	B-ISDN User Network Interface	ITU-T 03/93
I.432.1	B-ISDN User Network Interface Physical Layer Specification - General Characteristics	ITU-T 08/96
I.432.2	B-ISDN User Network Interface Physical Layer Specification for 155 520 kbit/s and 622 080 kbit/s	ITU-T 08/96
I.610	B-ISDN Operation and Maintenance Principles and Functions	ITU-T 11/95.
I.731	Types and General Characteristics of ATM Equipment	ITU-T 03/96.
I.732	Functional Characteristics of ATM Equipment	ITU-T 03/96
G.707	Network node interface for the SDH	ITU-T 03/96
G.803	Architectures of transport networks based on the SDH	ITU-T 03/93
G.804	ATM Cell Mapping into Plesiochronous Digital Hierarchy	ITU-T 11/93
G.805	Generic Functional Architecture of Transport Networks	ITU-T 11/95
G.810	Considerations on Timing and Synchronization Issues	ITU-T 08/96
G.957	Optical interfaces for equipments and systems relating to the SDH	ITU-T 07/95

ATM-Forum implementation agreements

af-phy.	UNI 3.1	ATM-Forum
af-phy.0015.000	ATM Physical Medium Dependent Interface Specification for 155 Mb/s over Twisted Pair Cable	ATM-Forum

4.4.4 Cross-Connect

Cross-connection method	Synchronous time slot interleaving
Frame frequency	8 kHz

Capacity:

The sum of cross-connected signals	64 Mbit/s (Basic Nodes and Mini Nodes) 8 x 64 Mbit/s = 512 Mbit/s (Cluster node)
Smallest cross-connect unit	64 kbit/s (Cluster Node) 8 kbit/s (single and double subrack node)

Signalling cross-connection	n x 500 bit/s (Channel Associated Signalling = CAS)	
Delay of cross-connect core:	n x 64 kbit/s	CAS bits (500 bit/s)
single and double subrack	1 frame = 125 µs	2 ms
Cluster node	2 frames = 250 µs	2 ms

Cross-Connect Delay Between Framed Interfaces (GMH):

n x 8 kbit/s, n x 64 kbit/s	< 600 µs (normal 2 frames interface buffer)
500 bit/s CAS	< 7 ms

Time integrity between the time slots in cross-connected signals is maintained.

4.4.5 Node Timing

Node master clock frequency	16 896 kHz ± 30 ppm (2 x 8448 kHz)
Master clock functional modes	Locking to the interface Rx clock (n x 64 kbit/s) Locking to external clock input (n x 64 kHz) Internal mode Clock fallback list (5 levels + internal mode)
Locking frequency	n x 64 kHz ± 50 ppm
External clock input	Frequency n x 64 kHz, n = 1…132 Electrically G.703
External clock output	Frequency 2048 kHz or 8448 kHz Locked to node master clock Electrically G.703
Connector type	75 Ω, SMB type connector (not in Mini Nodes) 120 Ω, D type 9-pin female connector
Jitter transfer function and jitter in the output clock	G.736

4.4.6 G.704 Framed Interface

4.4.6.1 Frame and Multiframe Buffer

Frame Buffer Mode[a]	Bit Rates	Rx Delay Frames	Tx Delay Frames	Main Usage
2 Fr	2 Mbit/s, 8 Mbit/s	0…2	0	trunk lines
4 Fr	n x 64 k, 2 Mbit/s, 8 Mbit/s	1…3	1	non-trunk lines and n x 64 kbit/s trunks
8 Fr	n x 64 k, 2 Mbit/s	2…6	1	split trunk lines
8 Fr	n x 64 k, 2 Mbit/s, 8 Mbit/s	1…7	1	
64 Fr	n x 64 k, 2 Mbit/s	1…63	1	plesiochronous buffer

a 1 Fr = 125 µs

Slip rate when the incoming signal is plesiochronous:

Buffer Length	Slip Rate n x 64 kbit/s	Slip Rate 2 Mbit/s	Slip Rate 8 Mbit/s
2 Fr	-	240/df	1024/df
4 Fr	n x 8/df[a]	256/df	1056/df
8 Fr (split trunk line)	2 x n x 8/df	512/df	-
8 Fr	4 x n x 8/df	1024/df	4224/df
64 Fr	32 x n x 8/df	8192/df	-

a df = frequency difference (input x Mbit/s signal frequency - nodes x Mbit/s frequency)

Split trunk line operation (many physical lines combined to one logical trunk):

— Line bit rates: n x 64 kbit/s ($3 \leq n \leq 32$), 2 Mbit/s
— All split components must have the same bit rate
— Tolerated delay difference between lines < 50 µs

Multiframe buffer modes:

When Frame Buffer Is	MFr Buffer[a]	Rx Delay	Tx Delay
2 frames long	2 MFr	0…2 MFr	0 Fr
4…8 frames long	2 MFr	0…2 MFr	1 Fr
64 frames long	4 MFr	1…3 MFr	1 Fr

a 1 MFr = 2 ms

Jitter and wander tolerance: G.823

4.4.6.2 8448 kbit/s Interface (CCITT G.704)

Electrical interface	G.703 Optical line
Multiplexing method	Synchronous time slot interleaving (G.704)
Bits in time slot	8
Time slots in frame	132 numbered 0…131
Frame alignment time slot	TS0/B1…8 + TS66/B1…6
Frame alignment procedure	G.744
Far-end alarm	TS66/B7
CRC error check	CRC-6 in bits TS99/B1…6 (can be disconnected)
CRC error indication to the remote end	TS99/B7
Error performance monitoring	G.821
Signalling multiframe time slots	TS67, 68, 69, 70 (G.704)
Multiframe time slot content	F0/TS sig (0000 xyxx)
Multiframe far-end alarm	F0/TS sig/B6
Multiframe alignment procedure	G.732 (same as in 2 Mbit/s interface) Separate multiframe alignment for each signalling time slot
Frames in multiframe	16
Signalling bits	4 pcs a, b, c, d /64 kbit/s time slot 2 pcs a, b / c, d /32 kbit/s 1 pc a/b/c/d /16 kbit/s
Control channel datalink	n x 8 kbit/s (n = 1…8) Any time slot except TS0 and TS66 DXX trunk lines preferable TS01/B1…B8 (64 kbit/s) TS33/B1…B8

Time slot usage in trunks

cross-connectable time slots with signalling bits (CAS)	120 time slots TS5…TS32, TS34…TS65 TS71…TS98, TS100…TS131
cross-connectable time slots without signalling bits	5 time slots TS1…TS4, TS33
free bits	TS66/B8 TS99/B8

4.4.6.3 2048 kbit/s Interface (CCITT G.704/706)

Electrical interfaces	G.703 (see Data Interface Modules) Line terminal Optical line V.35 V.36/V.11
Multiplexing method	Synchronous time slot interleaving
Bits in time slot	8
Time slots in frame	32 numbered 0…31
Frame alignment time slot	TS0
Frame alignment method	G.706
Far-end alarm	TS0/B3
CRC error check	CRC-4 in CRC multiframe of TS0/B1 (G.704/706, CRC can be disconnected)
CRC block error indication to the remote end	CRC multiframe E bit
Error performance monitoring	G.821
Signalling multiframe time slot	TS16 (G.704)
Multiframe alignment time slot content	F0/TS16 (0000 xyxx)
Multiframe far-end alarm	F0/TS16/B6-
Multiframe alignment method	G.732
Frames in multiframe	16
Signalling bits	4 pcs a, b, c, d /64 kbit/s time slots 2 pcs a, b / c, d /32 kbit/s 1 pc a/b/c/d /16 kbit/s

Time slot usage in trunks:

cross-connectable time slots with signalling bits (CAS)	30 time slots, TS1…TS15, TS17…TS31
free bits	TS0/B4…8 (see control channel datalink)
Control channel datalink	n x 8 kbit/s (n = 1…8) Any time slot except TS0 frame alignment bits DXX trunk lines preferable TS0/B5(8…16 kbit/s)

4.4.6.4 N x 64 kbit/s Interface with G.704 Type Frame

Electrical interface

n x 64 kbit/s baseband interface	see “Data Interface Modules” on page 96
1088 kbit/s Line terminal	
V.35n x 64 kbit/s	signals 103, 104, 113, 115 (V.35 electrical specs.)
V.36n x 64 kbit/s	signals 103, 104, 113, 115 (V.11 electrical specs.) for V.35 and V.36 n = 2…32, with n = 32
Multiplexing method	Synchronous time slot interleaving
Bits in time slot	8
Time slots in frame	n numbered 0…n-1
Frame alignment time slot	TS0
Frame alignment method	G.706
Far-end alarm	TS0/B3
CRC error check	CRC-4 in CRC multiframe of TS0/B1 (G.704/706, CRC can be disconnected)
CRC block error indication to the remote end	CRC multiframe E bit
Error performance monitoring	G.821
Signalling multiframe time slot (TS sig.)	Last time slot in frame (TSn-1) except with n ≥ 17 TS sig. = 16
Multiframe alignment time slot content	F0/TS sig. (0000 xyxx)
Multiframe far-end alarm	F0/TS sig./B6
Multiframe alignment method	G.732
Frames in multiframe	16
Signalling bits	4 pcs a, b, c, d /64 kbit/s 2 pcs a, b / c, d /32 kbit/s 1 pc a/b/c/d /16 kbit/s

Time slot usage in trunk lines:

cross-connectable time slots with signalling bits (CAS)	n-2 pcs
free bits	TS0/B4…8 (see control channel datalink)
Control channel datalink	n x 8 kbit/s (n = 1…8) Any time slot except TS0 frame alignment bits DXX trunk lines preferable TS0/B5(8 …16 kbit/s)

4.4.7 1544 kbit/s Interface

Electrical	G.703/ACCUNET T1.5
Bits in Timeslot	8 bits clear channel, 7 bits with signalling enabled
Time Slots in frame	24
Frame Alignment Method	TR-NWT-000170/G.706 Superframe and Extended Superframe
Yellow alarm	Superframe- Bit 2 all channels set to 0 or last Fs bit set to ‘1’ Extended Superframe- Repetative 8 ‘0’s, ‘1’s in datalink
CRC error check	CRC-6 as per TR-NWT-000499
Error performance monitoring	TR-NWT-000820
Frames in Multiframe	Superframe -12 Extended Superframe -24
Control Channel datalink	a n*8bits (n=1...8) in any channel time slots b ESF Datalink (4kbit/s)

4.4.8 Unframed Data Interfaces

4.4.8.1 V.24/V.28, V.35, V.36/V.11 - 1.2(19.2 kbit/s, 48,5 6, n x 64 kbit/s

Interface type	V.24/V.28	V.35, V.36/V.11 V.24/V.28	V.35, V.36 V.24 (n = 1)
Data bit rate	1.2, 2.4, 4.8 7.2, 9.6 14.4, 19.2, 38.4 kbit/s	48, 56 kbit/s	n x 64 kbit/s n = 1, 2…32
Framing inside DXX network	V.110	V.110	-
Interface functions	V.24	V.24	V.24
Handshake signal transmission[a]:			
105/109	SB	SB	V.13
106	X	X	-
108/107	SA	SA	-
140/142	V.54	V.54	V.54

a SA, SB, X are bits in a V.110 frame

Electrical interface

V.24	V.28 for all signals
V.35	V.35 for signals 103, 104, 113, 114, 115, V.28 for other signals
V.36	V.28 for signals 140, 141 and 142, V.11 for other signals
Interface signals:	102, 103, 104, 105, 106, 107, 108, 109, 113, 114, 115, 140, 141, 142
Connector type:	
V.24	ISO 2110, D type 25-pin female connector
V.35	ISO 2593, D type 34-pin female connector
V.36	ISO 4902, D type 37-pin female connector
Test loops via data interface	RL, V.54 remote loop, (loop 2); LL, V.54 local loop, (loop 3)

4.4.8.2 X.21 - 1.2(19.2 kbit/s, 48, 56, n x 64 kbit/s

Data bit rate	1.2, 2.4, 4.8, 9.6, 19.2, 38.4, 48 kbit/s	56 kbit/s	n x 64 kbit/s n = 1, 2,…32
Framing inside DXX network	X.30 (V.110)	V.110	-
Interface functions	V.24	V.24	-
Control signal transmission[a]			
C/I	S1 + S3 + S4	S3 + S4	-

a S1, S3, S4 are bits in a V.110 frame

Interface signals:

bit rates 1.2…48 kbit/s	G, T, R, S, C, I
bit rates 56…n x 64 kbit/s	G, T, R, S
Electrical interface	X.27 (V.11)
Connector type:	ISO 4903, D type 15-pin female connector

4.4.8.3 Transparent 2 Mbit/s, n x 64 kbit/s

Interface Type	G.703 2 Mbit/s	G.703 64 kbit/s	Opt. Line	Line Terminal	Baseband Line
Data bit rate, n x 64 kbit/s	n = 32	n = 1	n = 32	n = 17, 32	n x 64 kbit/s n = 1…12

4.4.9 GMU SDH Interface unit

GMU has three operating modes:

- terminal multiplexer (TM)
- terminal multiplexer with MS 1+1 protection (TM1+1)
- add-drop-multiplexer (ADM)

Trunk Interfaces

- STM-1 electrical, G.703
- STM-1 optical short-haul, G.957 (S-1.1)
- STM-1 optical long-haul, G.957 (L-1.1)
- 34 Mbit/s electrical, G.703

STM-1 electrical interface

Bit rate	155.52 Mbit/s
Input tolerance	±20ppm
Code	CMI
Nominal impedance	75 Ω
Pulse shape	G.703 figures 24 and 25
Maximum input attenuation	12.7 dB at 77.76 MHz (√f)
Jitter tolerance	G.825 § 4.1
Connector type	SMB (unbalanced 75 Ω)

STM-1 optical interface short-haul (S-1.1)

Bit rate	155.52 Mbit/s
Input tolerance	±20 ppm
Code	NRZ
Pulse shape	G. 957 fig. 2
Transmission path	Standard single-mode fibre (G.652 , G.957)
Optical transmitter	LASER multi-longitudinal mode transmitter
Operating wavelength range	1261 -- 1360 nm
Maximum spectral RMS width	7.7 nm
Mean launched power	
-minimum	-15 dBm
-maximum	-8 dBm
Minimum extinction ratio	8.2 dB
Optical receiver	PIN-diode
Receiver sensitivity (BER 1E-10)	-28 dBm
Receiver overload	-8 dBm
Connector type	SC or FC

STM-1 optical interface long-haul (L-1.1)

Bit rate	155.52 Mbit/s
Input tolerance	±20ppm
Code	NRZ
Pulse shape	G. 957 fig. 2
Transmission path	Standard single-mode fibre (G.652,G.957)
Optical transmitter	LASER multi-longitudinal mode transmitter
Operating wavelength range	1280…1335 nm
Maximum spectral RMS width	4 nm
Mean launched power	
-minimum	-5 dBm
-maximum	0 dBm
Minimum extinction ratio	10 dB
Optical receiver	PIN-diode
Receiver sensitivity (BER 1E-10)	-34 dBm
Receiver overload	-10 dBm
Connector type	SC or FC

S34M electrical interface

Bit rate	34.368 Mbit/s
Input tolerance	±20ppm
Code	HDB3
Nominal impedance	75 Ω
Pulse shape	G.703 figure 17
Jitter tolerance	G.823 § 3.1.1
Connector type	SMB (unbalanced 75 Ω)
Frame structure	G.832

Matrix 4/1

Matrix type	4-port T-S, strictly non blocking
Cross connection level	VC-2, VC-12
Connection types	unidirectional bi-directional loop
Connection capacity	4 x STM-1 port equivalent (two trunk ports, a tributary port and a monitoring port)
Delay	VC-12 from STM1 port to STM1 port less than 50 µs

Termination and mapping

Frame structures	STM-1, G.707 34 Mbit/s, G.832
Trail termination	VC-4 (east and west) P31s (G.832) (east and west) VC-2 x 10 VC-2-mc (m = 2 to 10) VC-12 x 32 VC-12-mc (m = 2 to 32)
Mapping	n x 64 kbit/s byte synchronous floating
SOH access	most SOH channels can be cross connected and accessed from other DXX interface units.
Concatenation	virtual concatenation of VC-2 and VC-12

Other characteristics

Clock generator	accuracy + 4.6 ppm
	holdover as in G.813
Clock source	STM-1, 2048 kbit/s, 2048 kHz
Line protection	Linear Multiplex Section 1+1
	Subnetwork Connection Non-intrusive 1+1 for VC-2, VC-12
Power supply	48 V DC
Power consumption	25 W
Unit size	76 x 160 x 233 mm (w x d x h)
Unit width	15 T

4.4.10 AIU ATM INTERFACE UNIT

4.4.10.1 ATM Access Interfaces

- STM-1 single mode fiber optical intraoffice, G.957
- STM-1 multimode fiber optical intraoffice, ATMF UNI3.1
- STM-1 UTP-5 cable electrical, ATMF af-phy.0015.000

STM-1 MMF Optical Interface Intraoffice

Bit Rate	155.52 Mbit/s
Input tolerance	±20 ppm
Code	NRZ
Pulse shape	ITU-T G.957 (fig.2)
Transmission media	multimode fiber
Optical transmitter	LED
Operating wavelength range	1261…1360 nm
Typical spectral RMS width	58 nm
Mean launched power: - minimum - maximum	 - 20 dBm - 14 dBm
Minimum extinction ratio	8.2 dB
Optical receiver	PIN diode
Receiver minimum sensitivity (BER 1E-10)	- 29 dBm
Receiver minimum overload	- 14 dBm
Connector type	SC

STM-1 SMF Optical Interface Intraoffice

Bit Rate	155.52 Mbit/s
Input tolerance	± 20 ppm
Code	NRZ
Pulse shape	ITU-T G.957
Transmission media	Singlemode fiber
Optical transmitter	Class-1 Laser (IEC825)
Operating wavelength range	1260…1360 nm
Typical spectral RMS width	7.7 nm
Mean launched power:	
- minimum	-15 dBm
- maximum	-8 dBm
Minimum extinction ratio	8.2 dB
Optical receiver	
Receiver minimum sensitivity (BER 1E-10)	- 28 dBm
Receiver minimum overload	- 8dBm
Connector type	SC

STM-1 UTP-5 Interface

Bit Rate	155.52 Mbit/s
Input tolerance	±20 ppm
Code	NRZ
Transmission media	UTP-5
Nominal impedance	100 Ω
Pulse shape	af-phy.0015.000
Jitter/Jitter tolerance	1.5ns peak-to-peak / af-phy.0015.000
Connector type	RJ-45/ISO/IEC 8877

ATM Cross Connect

Matrix type[a]	1:N
Cross-connection level	Virtual Path
Connection types	bi-directional
Connection capacity	16-32 Mbit/s
Maximum number of VPCs	256-1024
Buffering	Output buffered per ATM virtual trunk

a Cross-connection between ATM Access Interface (1) and ATM virtual trunks (N). VP Cross-connection between ATM virtual trunks is not supported.

ATM Access Interface Termination and Mapping

Frame structures	STM-1, G.707
ATM cell mapping	VC4, I.432.2 and G.707
SOH access	Limited

ATM Virtual Trunk Termination and Mapping

Frame structures	DXX interface unit framings
ATM cell mapping	Byte synchronous nx64k to X-bus

Other characteristics

Power supply	48 V DC
Power consumption	17 W
Unit size w x d x h (mm)	50x160x233
Unit width (T)	10

4.4.11 Data Interface Modules

8448 kbit/s, G.703 Interface (G703 module)

Bit rate	8448 kbit/s ±30 ppm
Coding	HDB3
Nominal peak voltage	2.37 V/75 Ω unbalanced
Pulse width	59 ns ±10 ns
Attenuation margin	0…6 dB/4 MHz
Jitter tolerance	G.823
Connector type	75 Ω, SMB connector

2048 kbit/s, G.703 Interface (G703 module)

Bit rate	2048 kbit/s ±50 ppm
Coding	HDB3
Nominal peak voltage	2.37 V/75 Ω unbalanced 3.0 V/120 Ω balanced
Pulse width	244 ns ±20 ns
Attenuation margin	0…8 dB / 1 MHz
Jitter tolerance	G.823
Connector type	75 Ω, SMB type connector 120 Ω, D-type 9-pin female connector

64 kbit/s, G.703 Interface (G703-64 module)

Bit rate	64 kbit/s ±50 ppm
Type	co- or contradirectional
Impedance	120 Ω balanced
Nominal peak voltage	1.0 V
Pulse width	244 ns ±20 ns
Attenuation margin	0…3 dB
Jitter tolerance	G.823
Connector type	D-type 15-pin female connector

2048 kbit/s,G.703 Interface (G703-75 module)

Bit rate	2048 kbit/s ±50 ppm
Code	HDB3 (G.703 Annex A)
Nominal impedance	75 Ω unbalanced
Pulse shape	G703 Figure 15
Nominal peak voltage	2.37 V (75 Ω)
Nominal pulse width	244 ±25 ns
Attenuation margin	6 dB at 1024 kHz
Input return loss	G.703 § 6.3.3
Output return loss	ETS 300 166 § 5.3
Jitter tolerance	G.823 § 3.1.1
Output jitter when transmit signal timing is supplied by the SXU operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)
Output jitter when the node is synchronized from an G703-75 interface or SXU external clock input interface	TBR 12 § 5.2.1.4
Output short circuit current	< 50mA RMS
Connector type	SMB

2048 kbit/s, G.703 Interface (G703-120 module)

Bit rate	2048 kbit/s ±50 ppm
Code	HDB3 (G.703 Annex A)
Nominal impedance	120 Ω balanced
Pulse shape	G703 figure 15
Nominal peak voltage	3.0 V (120 Ω)
Nominal pulse width	244 ±25 ns
Attenuation margin	6 dB at 1024 kHz
Input return loss	G.703 § 6.3.3
Output return loss	ETS 300 166 § 5.3
Jitter tolerance	G.823 § 3.1.1
Output jitter when transmit signal timing is supplied by the SXU operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)
Output jitter when node is synchronized from an G703-120 interface or SXU external clock input interface	TBR 12 § 5.2.1.4
Connector type	D-type 9-pin female connector

8448 kbit/s, G.703 Interface (G703-8M module)

Bit rate	8448 kbit/s ±30 ppm
Code	HDB3 (G.703 Annex A)
Nominal impedance	75 Ω unbalanced
Pulse shape	G.703 figure 16
Nominal peak voltage	2.37 V (75 Ω)
Nominal pulse width	59 ± 10 ns
Attenuation margin	6 dB at 4224 kHz
Input return loss	G.703 § 7.3.3
Jitter tolerance	G.823 § 3.1.1
Output jitter when transmit signal timing is supplied by the SXU operating in the internal mode	< 0.05 UI (20 Hz…400 kHz)
Connector type	SMB (unbalanced 75 Ω)

2048 kbit/s,G.703 Interface (G703-75-4CH module)

Bit rate	2048 kbit/s ±50 ppm
Code	HDB3 (G.703 Annex A)
Nominal impedance	75 Ω unbalanced
Pulse shape	G703 Figure 15
Nominal peak voltage	2.37 V (75 Ω)
Nominal pulse width	244 ±25 ns
Attenuation margin	6 dB at 1024 kHz
Input return loss	G.703 § 6.3.3
Output return loss	ETS 300 166 § 5.3
Jitter tolerance	G.823 § 3.1.1
Output jitter when transmit signal timing is supplied by the XCG operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)
Output jitter when the node is synchronized from an G703-75-4CH interface or XCG external clock input interface	TBR 12 § 5.2.1.4 TBR 13 § 5.2.1.4
Output short circuit current	< 50mA RMS
Connector type	SMB (unbalanced 75 Ω)
Overvoltage Protection	G.703 Annex B

2048 kbit/s, G.703 Interface (G703-120-4CH module)

Bit rate	2048 kbit/s ±50 ppm
Code	HDB3 (G.703 Annex A)
Nominal impedance	120 Ω balanced
Pulse shape	G703 figure 15
Nominal peak voltage	3.0 V (120 Ω)
Nominal pulse width	244 ±25 ns
Attenuation margin	6 dB at 1024 kHz
Input return loss	G.703 § 6.3.3
Output return loss	ETS 300 166 § 5.3
Jitter tolerance	G.823 § 3.1.1
Output jitter when transmit signal timing is supplied by the XCG operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)
Output jitter when node is synchronized from an G703-120-4CH interface or XCG external clock input interface	TBR 12 § 5.2.1.4 TBR 13 § 5.2.1.4
Connector type	D-type 9-pin female connector
Overvoltage Protection	G.703 Annex B

2048 kbit/s, G.703 Interface (G703-75-Q and G703-120-Q module)

Nominal impedance	75 Ω unbalanced/G703-75-Q	120 Ω unbalanced/G703-120-Q
Bit rate	2048 kbit/s ± 50 ppm	2048 kbit/s ± 50 ppm
Code	HDB3 (G.703 Annex A)	HDB3 (G.703 Annex A)
Pulse shape	G.703 figure 15	G.703 figure 15
Nominal peak voltage	2.37 V	3.0 V
Nominal pulse width	244 ± 25 ns	244 ± 25 ns
Attenuation margin	6 dB at 1024 kHz	6 dB at 1024 kHz
Input return loss	G.703 § 6.3.3	G.703 § 6.3.3
Output return loss	ETS 300 166 § 5.3	ETS 300 166 § 5.3
Jitter tolerance	G.823 § 3.1.1	G.823 § 3.1.1
Output jitter when transmit signal timing is supplied by the SXU/XCG operating in the internal mode	<0.05 UI (20 Hz…100 kHz)	<0.05 UI (20 Hz…100 kHz)
Output jitter when the node is synchronized from any 2048 Mbit/s G.703 interface or SXU/XCG external clock input interface	TBR 12 § 5.2.1.4 TBR 13 § 4.2.1.4	TBR 12 § 5.2.1.4 TBR 13 § 4.2.1.4
Output short circuit current	<50mA RMS	
Connector type	SMB	D-type 9-pin female connector

4.4.12 2048 kbit/s and 1088 kbit/s Line Terminal Interface (LTE Module)

Bit rate	2048 kbit/s ± 50 ppm	1088 kbit/s ±50 ppm
Coding	HDB3	HDB3
Nominal peak voltage	3.0V / 120 Ω symmetrical	
Pulse width	244 ns ±25 ns	460 ns ±40 ns
Attenuation margin	0…36 dB at 1024 kHz	0…36 dB at 544kHz
Jitter tolerance	G.823	Mask like G.823 for 2048 kbit/s with the following exceptions: A019.6 (18 µs) A10.75 A20.10 f450 kHz
Input impedance	120 Ω symmetrical	
Return loss	G.703	
Connector type	D type 9-pin female connector	
Overvoltage protection	Gas discharge tubes, diodes	

4.4.12.1 Optical Line Interface 2048 kbit/s/8448 kbit/s, LED and Laser (OTE-LED and OTE-LP Modules)

Bit rate		2048 kbit/s ±50 ppm 8448 kbit/s ±30 ppm	
Transmission path		Standard multi mode fiber (G.651) Standard single mode fiber (G.652)	
Optical transmitter		Semiconductor LED or Laser	
Nominal wave length		1300 nm	
Functional Mode		Minimum Output Power	Attenuation Margin
OTE-LED:			
multi mode	LED 2 M	-20 dBm	30 dB
single mode	LED 2 M	-30 dBm	20 dB
multi mode	LED 8 M	-20 dBm	22 dB
single mode	LED 8 M	-30 dBm	12 dB
OTE-LP:			
multi mode	Laser LP 2 M	-2 dBm	48 dB
single mode	Laser LP 2 M	-4 dBm	46 dB
multi mode	Laser LP 8 M	-2 dBm	40 dB
single mode	Laser LP 8 M	-4 dBm	38 dB
Optical line code		CMI	
Symbol rate		4096 kBaud (2 Mbit/s) 16896 kBaud (8 Mbit/s)	
Optical receiver		PIN diode	
Min. sensitivity (BER 10 -9)		-50 dBm (2 M) -42 dBm (8 M)	
Optical connector		FC-type with a receptacle	

4.4.12.2 Baseband Line Interface 2.4…19.2 kbit/s, 48, 56…384 kbit/s (BTE-64 and BTE-384 Modules)

Bit rate	2.4, 4.8, 7.2, 9.6, 14.4, 19.2, 8, 16, 32, 48, 56, 80, n x 64 kbit/s (n = 1…6)
Line interface	2/4 W full-duplex
Line code	biphase space
Interface impedance	150 Ω symmetrical (BTE-384) 820 Ω parallel with 180 Ω + 82 nF (BTE-64)
Output level/150 Ω	0/-6 dBm
Return loss	> 12 dB
Maximum input level/150 Ω	0 dBm
Minimum input level/150 Ω	BTE-64: -30 - -38 dBm (varies according to bit rate) BTE-384: -33 - -38 dBm (varies according to bit rate)
Equalizer	adaptive
Connector type	D type 9-pin female connector

4.4.12.3 Baseband Line Interface 256…768 kbit/s (BTE-768 Module)

Bit rate	n x 64 kbit/s, n = 4…12
Line interface	4 W full-duplex
Line code	Partial response, class 4, seven levels
Interface impedance	150 Ω symmetrical
Output level/150 Ω	+6 dBm/0 dBm
Return loss	> 12 dB
Maximum input level/150 Ω	+6 dBm
Minimum input level/150 Ω	-25 dBm
Equalizer	adaptive
Connector type	D type 9-pin female connector

4.4.12.4 Baseband Line Interfaces 320…4224 kbit/s (BTE-1088, 2048, 2048-2W and 4096 Modules)

Bit rate	n x 64 kbit/s, n = 5, 9,17 (BTE-1088) n=16,17, 32,33 (BTE-2048) n=16,17,32,33,64,66(BTE-4096)
Line interface	4 W full-duplex (BTE-2048-2W also 2W full-duplex)
Line code	2B1Q
Interface impedance	135 Ω symmetrical
Output level/135 Ω	+13.5 /+6 dBm/0 dBm
Return loss	> 12 dB
Maximum input level/135 Ω	+ 15 dBm
Minimum input level/135 Ω	- 30 dBm
Equalizer	adaptive
Connector type	D type 9-pin female connector

4.4.12.5 Baseband Line Interfaces 320…2304 kbit/s (BTE-320, 576, 1088-2W and 2304 Modules)

Bit rate	n x 64 kbit/s n = 5 (BTE-320) n=5, 9 (BTE-576) n=5, 9, 16, 17 (BTE-1088-2W) n=16, 17, 32, 33, 34, 36 (BTE-2304)
Line interface	2W full-duplex (BTE-1088-2W and BTE-2304 also 4W full-duplex)
Line code	2B1Q
Interface impedance	135 Ω symmetrical
Output level/135 Ω	+13.5 /+6 dBm/0 dBm
Return loss	> 12 dB
Maximum input level/135 Ω	+ 15 dBm
Minimum input level/135 Ω	- 30 dBm
Equalizer	adaptive
Connector type	D type 9-pin female connector

4.4.12.6 Baseband Line Interfaces 160 kbit/s (IUM-5T and IUM-10T)

Line rate	160 kbit/s (2B+D)
Symbol rate	80 kbaud
Line interface	2 W full-duplex
Line code	2B1Q
Interface impedance	135 Ω symmetrical
Output level/135 Ω	+13.5 dBm
Return loss	Defined in ANSI T1.601-1992 1 ... 10 kHz:> 0 ... 20dB 10 ... 25 kHz:> 20dB 25 ... 250 kHz:> 20 ... 0 dB
Connector type	Modular 8-pin RJ-45 jack connector

4.4.12.7 1544 kbit/s (T1) Interface

Bit Rate	1.544MBits/S +/- 50 ppm
Coding	AMI AMI with zero code suppression B8ZS
Nominal Peak Voltage	3V
Nominal Pulse Width	323nS
Attenuation	20dB
Line Buildouts	0dB -7.5dB -15dB -22.5dB
Jitter	AT&T TR62411 (ACCUNET T1.5 Service). Jitter tolerance and transfer function also depend on the node main PLL. Currently max jitter amplitude in frequency range 1-120Hz is 24 UI.
Connector type	D-type 15 pin female
Termination	100 Ω

4.4.12.8 ISDN U-Interface Unit (ISD-LT/NT)

General features:

Number of channels	4
Channel capacity available to NTU user	2B+D + overhead, 160kbit/s, “semitransparently through DXX Network”

Line interface:

Line rate	160 kbit/s (2B + D)
Symbol rate	80 kBaud
Signal encoding	2B1Q
Impedance	135 Ohm
Line connection	2-wire full duplex
Frame structure	ETR 080
Line monitoring in DXX mode	1. Dying gasp monitoring 2. Carrier detection 3. Bit error rate (calculated from CRC)
Line power feeding	Five voltage levels: OFF, 60V, 68V, 95V, 100V, 110V Max. feeding current is 25 mA

Performance:

Exceeds ETSI ISDN U-interface (ETR 080 1993) performance requirements for 2-pair 2B1Q-systems line rate 160 kbit/s.

Max. cable attenuation	better than 40 dB at 40 kHz
Max cable length	about 8 km (0.5 mm/40 nF/km cable , no noise) about 5 km (0.4 mm/46 nF cable, no noise) (guidelines only: actual length depends on cable characteristics)

Diagnostics:

Loops	Interface-loop, data is looped back to XBUS on interface module Equipment loop, data is looped back to XBUS on base unit Line loop, data is looped back to line on base unit The use of loops are is relevant generallybasically in ISD-LT DXX mode only
Operation	ETR080, G.960, G.961
Statistics	G.821

4.4.12.9 ECS X.50 Server

Customer Data Rates Supported

V.110	600,1200,2400,4800,9600,14400,19200,48000 bits/s
V.110M	600,1200,2400,4800,9600,14400,19200,48000 bits/s
X.50 Division 201.11.96	600,1200,2400,4800,9600,14400,19200,48000 bits/s
X.50 Division 3	1200,2400,4800,9600,14400,19200,48000 bits/s
X.50bis	48000 bits/s

ECS Capacity

Number of X.50 bearer channels per unit:8 for 10T, 4 for 5T

Number of V.110 channels per unit:60 for 10T, 30 for 5T

X.50 Capacity

Number of X.50 channels per bearer for customer data rate

600 bits/s	80 (not available in X.50 Division 3)
1200 bits/s	40 (if X.50 Division 3 this is allocated as 2400 bits/s and only 20 channels are available)
2400 bits/s	20
4800 bits/s	10
9600 bits/s	5
14400 bits/s	2
19200 bits/s	2
48000 bits/s	1

Octet Assignments

Valid X.50 octet assignments for customer data rate.

600 bits/s	1 through 80
1200 bits/s	1 & 41, or 2 & 40, or 3 & 43, or ... 40 & 80
2400 bits/s	1 through 20 (see note)
4800 bits/s	1 & 11, or 2 & 12, or ... 40 & 80 (see note)
9600 bits/s	1 & 6 & 11 & 16, or 2 & 7 & 12 &, or ... 5 & 10 & 15 & 20 (see note)
14400 bits/s	1 & 2 & 6 & 11 & 12 & 16 or 3 & 4 & 8 & 13 & 14 & 18 (see note)
19200 bits/s	1 & 2 & 6 & 7 & 11 & 12 & 16 & 17, or 3 & 4 & 8 & 9 & 13 & 14 & 18 & 19, or 1 & 3 & 6 & 8 & 11 & 13 & 16 & 18, or 2 & 4 & 7 & 9 & 12 & 14 & 17 & 19, or 3 & 5 & 8 & 10 & 13 & 15 & 18 & 20 (see note)
48000 bits/s	All

NOTE!

Octet assignments reflect ITU-T Recommendation X.50 Division 3 (20 octets). If an X.50 bearer has been configured as X.50 Division 2 (80 octets), the listed subrate channels octets shall be continued throughout the 80 octet frame. For example a 9600 bits/s channels shall reside in the following octets: 1 & 6 & 11 & 16 & 21 & 26 & 31 & 36 & 41 & 46 & 51 & 56 & 61 & 66 & 71 & 76.

X.50 Interface Requirements

The X.50 bearer channel may connected to any Nx64kbit/s data interface. Byte alignment is not required except for 48kbit/s X.50 bis channels.

Faults detected and reported

X.50 AIS
X.50 Loss of Frame Alignment
X.50 Frame Far-End Alarm (RAI)
X.50 Unavailable state in terms of G.821
X.50 Performance Event
X.50 Excessive error ratio 10^{-4}, 10^{-5}, and 10^{-6}
X.50 Bearer in Loopback
V.110 Frame Far-End Alarm (RAI)
V.110 AIS
V.110 Loss of Frame Alignment
V.110 Unavailable state in terms of G.821
V.110 Channel in Loopback
V.110 Performance Event
Note: Faults may be masked on X.50 bearers and V.110 channels.

V.110 Line conditioning options available for X.50 faults

- AIS (all 1’s, no framing) shall be sent on all V.110 channels associated with the X.50 channel.
- IDLE (all 1’s, valid framing) shall be sent on all V.110 channels associated with the X.50 channel.
- IDLE (all 1’s, valid framing) followed by Network Out of Service (NOS - SB=1 data = 0) shall be sent on all V.110 channels associated with the X.50 channel.

X.50 Line conditioning options available for V.110 faults

- Network Out Of Service (NOS - S=OFF, DATA=0) shall be sent on the X.50 octet(s) associated with the V.110 channel.
- IDLE (S=OFF, DATA=1) followed by NOS (S=OFF, DATA=0) shall be sent on the X.50 octet(s) associated with the V.110 channel.

Diagnostics available on ECS Module

X.50 External Line Loopback
V.110 External Line Loopback
X.50 Internal Line Loopback
V.110 Internal Line Loopback
Patterned Local Loopback (module self test)

4.4.13 VF & EM Interface 64 kbit/s PCM and 32 kbit/s ADPCM

Voice Frequency Interface

Number of VF channels per unit	5, 10, 20	
Type of encoding	64 kbit/s PCM CCITT G.711 A-law 32 kbit/s ADPCM CCITT G.721 24 kbit/s ADPCM ANSI T1.303 16 kbit/s ADPCM by Dallas Semiconductor	
Type of VF interface	2- or 4-wire	
4-wire VF characteristics	G.712/G.714	
2-wire VF characteristics	G.713/G.715	
Nominal impedance	600 Ω	
Return loss 300-3400 Hz	> 20 dB	
Terminal balance return loss	> 18 dB	
Relative levels	4-wire	2-wire
input	-16 dBr…0 dBr	-10 dBr…0 dBr
output	-16 dBr…+6 dBr	-16 dBr…-2 dBr
adjustability	0.1 dB steps	

Longitudinal balance	> 60 dB
Out-of-band signals at channel output	< -30 dB
Discrimination against out-of-band input signals	> 30 dB
Absolute channel delay @ 1 kHz	
VF to PCM	< 600 µs
PCM to ADPCM	< 375 µs
ADPCM to PCM	< 375 µs
PCM to VF	< 500 µs
Total distortion (CCITT G.712/G.713 method 1)	
64 kbit/s PCM	G.712/G.713
32 kbit/s ADPCM	G.712/G.713
24 kbit/s ADPCM	G.712/G.713 - 5 dB
16 kbit/s ADPCM	G.712/G.713 - 13 dB
Idle channel noise	
-64 kbit/s PCM	< 75 dBm0p

EM Signalling Interface

Polarity	negative
Input/output state	
closed	binary 0
open	binary 1
Signalling distortion	< 3 ms
ADPCM processing	G.761
Earth potential offset	< + 2 V
Test point	uP interface to each signalling bit
Output	
closed state resistance	< 50 Ω
open state resistance	> 200 kΩ
closed state voltage (I < 75 mA)	< 2 V
voltage transients (< 5ms)	< 180 V
open state current	< 50 µA
closed state current	< 75 mA
current transients (< 10 ms)	< 100 mA
digital noise filtering	RC = 10 ms
Input	
closed state current	< 10 mA
open state voltage	-10 V
noise filtering	RC = 40 µs
Cable characteristics	
series resistance	< 350 Ω
resistance to earth	> 20 kΩ
capacitance to earth	< 0.3 µF

4.4.14 Telephone Interfaces (CCO and CCS)

Transmission Characteristics

Number of channels per unit	10	
Type of encoding	64 kbit/s PCM (CCITT G.711 A-law) 16, 32 kbit/s ADPCM (ITU-T G.726)	
VF characteristics	G.712	
Nominal impedance	275Ω + 850 Ω//150 nF	
Return loss 300Hz…600Hz	>15 dB	
Return loss 600Hz…3400Hz	> 20 dB	
Terminal balance return loss (TBRL)	> 20 dB	
Relative levels		
input	-12 dBr…+1 dBr	
output	-16 dBr…+1 dBr	
adjustability	0.1 dB/steps	
Longitudinal balance		
CCO	> 50 dB	
CCS	> 40 dB	
Out-of-band signals at channel output	< -30 dB	
Absolute channel delay @ 1 kHz		
VF to PCM	< 700 µs	
PCM to VF	< 700 µs	
PCM to ADPCM	< 400 µs	
ADPCM to PCM	< 400 µs	
Total distortion (CCITT G.712/G.713 method 1)		
64 kbit/s PCM	G.712	
Idle channel noise		
64 kbit/s PCM	< -75 dBmOp	
Noise in conversation state	CCO	CCS
input	< -66 dBmOp	< -64 dBmOp
output	< -75 dBmOp	< -67 dBmOp

DC Characteristics For Extension Unit, CCS

Voltage feed	
quiescent condition	48 Vdc + 20 %/-15 %
Current feed	
off-hook condition	48/(1650 + R) A min. 52/(1550 + R) A max. (R = 0…1800)
short circuit between a, b and earth, any combination	150 mA max.
Extension line resistance	
loop resistance including a telephone set in off-hook condition	1800 Ω max.

Signalling Characteristics For Extension Unit, CCS

Signalling states detection	
on-hook condition loop current	3 mA max.
off-hook condition loop current	10 mA min.
multifrequency signalling	transparently to PBX
loop disconnect signalling	supported
Ringing signal	
frequency	25 Hz +/- 4 %
distortion	10 % THD
voltage:	
no load	75 V rms. max.
at terminals across 5.2 kΩ	52 Vrms. min.

Loop Termination for PBX Unit, CCO

PBX line interface	
high-ohmic condition	1 MΩ min.
low-ohmic condition	350 Ω max.
ringing signal detector impedance at 25 Hz	8 kΩ min
loop DC current	13 mA min. 40 mA max.

Signalling Characteristics for PBX Unit, CCO

ringing signal to be detected	30 V rms. min.
ringing signal frequency	25 Hz +/-12%
50 Hz ringing signal detection	supported
ringing signal not to be detected	10 V rms. max.

4.4.15 Voice/Fax Compression

Voice coder specifications		
Type of encoding	16 kbit/s ATC	
	8 kbit/s CELP	
Signal/noise ratio	> 30 dB	
(1004 Hz @ 0 dBm0 single tandem, single tone)		
Magnitude transfer response		
(1004 Hz @ 0 dBm0)	600 - 3500 Hz	+/- 0.5 dB
	300 - 3500 Hz	+/- 1.5 dB
	100 - 3900 Hz	+/- 15 dB
Fax rates supported		
16 kbits/s	V.21 300 bit/s	
	V.27 ter 2400 bit/s	
	V.27 ter 4800 bit/s	
	V.29 7200 bit/s	
	V.29 9600 bit/s	
8 kbit/s	V.21 300 bit/s	
	V.27 ter 2400 bit/s	
	V.27 ter 4800 bit/s	
	V.29 7200 bit/s	
Data modem rates supported		
16 kbit/s	V.22 1200 bit/s	
	V.22bis 2400bit/s	
	bell 103 300 bit/s	
8 kbit/s	none	
End-to-end delay		
16 kbit/s	less than 80 ms	
8 kbit/s	less than 150 ms (excluding delays of transmission links)	
Echo canceller		
End path cancellation	32 mS	
DTMF detection		
frequency deviation	+/- 1.4 % max. of nominal	
level range	0 to - 25 dBm	

pulse duration	40 mSec minimum	
interdigit duration	40 mSec minimum	
pulse interval (pulse on+pulse off)	93 mSec minimum	
DTMF regeneration		
frequency deviation	+/- 0.5 % of nominal	
level range	+/- 3 dB (of detected valid level)	
Tone generation		
frequency accuracy	1020/1000 Hz	+/- 0.5%
level accuracy	1020/1000Hz	+/- 0.5 dB
Tone detection		
frequency accuracy	+/- 0.5%	
frequency resolution	1 Hz	
level range	0 to - 45 dBm	
level accuracy	+/- 0.5 dB	
level resolution	0.1 dB	

4.4.16 Management and Alarm Interfaces

Service Computer (SC) Interface

Interface type	V.24
Electrical interface	V.28
Data bit rate	9.6 kbit/s asynchronous
Character format	8 bit, no parity, 1 stop bit
Connector type	ISO 2110, D type 25-pin female connector
Interface signals	102, 103, 104, 105, 106, 107, 108, 109
Protocol	Layers 2…7 proprietary

Management Computer (SCC) Interface)

Interface type	X.21	
Electrical interface	X.27 (V.11)	
Data bit rate	64 kbit/s synchronous	
Connector type	ISO 4903, D type 15-pin male connector	
Interface signals	G, T, R, S, C, I	
Protocol	Layer 2	X.25 LABP
		X.25 PLP
	Layer 3…7	proprietary

Equipment Alarm Outputs PMA, DMA, MEI

Three alarm outputs:	
PMA	Nodes prompt maintenance alarm (ITU-T)
DMA	Nodes deferred maintenance alarm (ITU-T)
MEI	Nodes maintenance event information (ITU-T)
No alarm state:	
Contact resistance	> 100 kΩ
Voltage	-100…+100 V
Alarm state:	
Contact resistance	< 50 Ω
Current	-100…+100 mA
Connector type	D type 9-pin male connector

Output contacts are floating and the other end can be tied to the equipment earth.

4.4.17 Power Supply

DC Power Supply

Input voltage	30…60V Positive pole earthed, can be duplicated /protected
Battery interface	CEPT Rec. T/TR 02-02
Connector type	D type 3W3 male connector

AC Power Supply

Input voltage (DXX and NTUs)	230 VAC +6/-15 % 47…63 Hz
Input voltage (SBM 2048M)	110…240 VAC +10/-10 % 47…63 Hz

Power Consumption of Nodes

Basic and Cluster node	< 100 W / one shelf (2 Mbit/s G.703 interfaces)

Power Consumption of Network Elements

Module/Unit	Description	Power Consumption (max)
ADPCM-10VF	Voice frequency interface module for CAE	3.0W
AIU 1:1	ATM Interface Unit	17W
AIU 1:4	ATM Interface Unit	17W
ALARM-IF	Alarm interface module	0.1W
BBU	Battery backup unit	0.5W
BCU	Battery charger unit	2.5W
BOU	Battery output unit	1.0W
BTE-64	Baseband interface module	3.3W
BTE-384	Baseband interface module	3.3W
BTE-768	Baseband interface module	4.3W
BTE-1088	Baseband interface module	4.3W
BTE-2048	Baseband interface module	5.0W
BTE-2048-2W	Baseband interface module	4.5W
BTE-4096	Baseband interface module	5.0W
CAE	Voice frequency interface unit	5.0W
CCU	Cluster node control unit	5.0W
CCO	PBX interface unit	10W
CCS	Extension interface unit	50W
CXU-A	Cluster node cross-connect unit / Slave	14W
CXU-M	Cluster node cross-connect unit / Master	8.0W
CXU-S	Cluster node signalling cross connect unit	14W
EAE	PCM/ADPCM server	7.0W
EM-2*10	E&M signalling module for CAE	2.0W

Module/Unit	Description	Power Consumption (max)
ECS-5T	V.110 to X.50 conversion server unit	6.5W
ECS-10T	V.110 to X.50 conversion server unit	10.5W
EPS-10T	Fax/Voice compression unit	17W
EPS-5T	Fax/Voice compression unit	9.0W
G703	G.703 interface module for GMH	1.7W
G703-8M	G.703 8448kbit/s interface module	1.0W
G703-64	G.703 64 kbit/s interface module	1.5W
G703-75	G703 75 Ω interface module	1.0W
G703-120	G.703 120 Ω interface module	1.0W
G703-75-4CH	G.703 75 Ω 4 Channel Interface module	3.5W
G703-120-4CH	G.703 120 Ω 4 Channel Interface module	3.5W
G703-75-Q	G.703 75 Ω 4 Channel Interface module	3.0W
G703-120-Q	G.703 120 Ω 4 Channel Interface module	3.0W
G703-PDA	PDA interface module	1.5W
GCH-A	Unframed data interface unit	3.0W
GMH	Framed interface unit	4.0W
GMM+T1	T1 interface unit	5.0W
GMU	SDH interface unit	17W
GMU-M	SDH interface unit	17W
HDLC-4CH	Control channel expansion module	1.0W
ISD-LT	ISDN U-Interface Unit	11W (without line load)
ISD-NT	ISDN U-Interface Unit	5.6W
IUM-5T	Baseband interface unit	5.5W
IUM-10T	Baseband interface unit	7.0W
LTE	Line terminal 1/2 Mbit/s	1.1W
OTE-LED	Optical line interface module 2/8 Mbit/s	3.7W
OTE-LP	Optical line interface module 2/8 Mbit/s	5.4W
PAU	Power Supply Unit	65W
PAU-5T	Power Supply Unit	24W
PCM-10VF	PCM interface module	3.0W
PCU	Power control unit	1.0W
PFU	Fuse Unit (-48V, old type)	5.0W
PFU-A	Fuse Unit (-48V)	5.0W
PFU-A-24V	Fuse Unit (+24V)	7.0W
PFU-B	Fuse Unit (-48V, protected use)	5.0W
PFU-B-24V	Fuse Unit (+24V, protected use)	7.0W
PMP-Server	PMP Server unit	3.5W
QMH	Framed interface unit, 4 channels	4.5W

Module/Unit	Description	Power Consumption (max)
SCC-IF	Control interface module	0.3W
SCU	Node control unit	5.0W
STM-1-E	Electrical interface module	4.1W
STM-1-LH-13	Optical short-haul module	2.6W
STM-1-SH-13	Optical long-haul module	2.6W
SXU-A	Cross-connect unit / small	8.0W
SXU-B	Cross connect unit / large	17W
SXU-C	Cluster slave subrack cross-connect unit	8.0W
SYN-34-E	Synchronous electrical interface module	1.7W
V24-DCE	V.24 interface module for VCM-5T-A	1.5W
V24-DTE	V.24/V.28 DTE interface module	1.5W
V24-PMP	V.24/V.28 PMP interface module for VCM-5T-A	1.5W
V35	V.35 interface module for VCM-10T-A	1.5W
V35-G704	V.35 interface module for GMH	1.5W
V35-G704-B	V.35 interface module for GMH	2.0W
V35-G704-BS	V.35 interface module for GMH	2.0W
V35-IEC	V.35 interface module for VCM-5T-A	1.5W
V36	V.36 interface module for VCM-10T-A	1.5W
V36-G704	V.36 interface module for GMH	1.5W
V36-IEC	V.36 interface module for VCM-5T-A	1.5W
VCM-10T-A	Unframed interface unit	3.5W
VCM-5T-A	Unframed interface unit	3.5W
VMM	Low overhead framed interface unit	4.5W
X21	X.21 interface module for VCM-5T-A	1.5W
X21-G704	X.21 interface module for GMH	1.5W
XCG	Cross-connect and control unit	12W

4.4.18 Mechanics

Basic and Cluster Node Dimensions and Weight

Basic node consists of one single or double subrack.

Cluster node consists of one double subrack and 1…8 single or double subracks.

Subrack/single	Wx D x H	451 x 255 x 310 mm	(19"/7 U subrack)
Subrack/double	W x D x H	451 x 255 x 620 mm	(19"/14 U subrack)
Air deflector plate	W x D x H	451 x 255 x 44 mm	(19"/1 U)
Unit	W x D x H	25 x 160 x 233 mm 50 x 160 x 233 mm 75 x 160 x 233 mm	(E2, 6 U/5 T) (E2, 6 U/10 T) (E2, 6 U/15 T)

An air deflector plate is recommended below each single/double subrack.

Subrack/single	< 15 kg	(19"/7 U subrack incl. units)
Subrack/double	< 30 kg	(19"/14 U subrack incl. units)

Midi Subrack Dimensions and Weight

2 x Midi Subrack	W x D x H	451 x 255 x 310 mm	(19"/7 U subrack)
Midi Subrack (single)	weight	< 10 kg	(incl. units)

4.4.19 DXX Products Usage Limitations

— GDH 230, G703 Interface Module (G.703 2Mbit/s, 8Mbit/s) should always be installed in EMC cabinet when 8Mbit/s is used.

— BTE-64 nor BTE-384 (version 2.0 or earlier) does not fulfill the test level 1 of ENV 50141 (1993), Conducted Disturbances Induced by Radio Frequency Fields; Immunity Test.

Digital interface modules GDH 507 (G703-8M) and GDH 476 (G703-75) are approved only for use with the following BABT certified models of DXX. Use of the product with a system not listed here may result in a hazard and will invalidate the BABT certification.

— DXX Basic Node

— DXX Cluster Node

— DXX Midi Node

The cards must be installed in accordance with the installation instructions provided.

Digital interface modules GDH 508 (G703-8M-M) and GDH 477 (G703-75M) are approved only for use with the following BABT certified models of DXX. Use of the product with a system not listed here may result in a hazard and will invalidate the BABT certification.

— DXX Mini Node

— DXX Micro Node

The cards must be installed in accordance with the installation instructions provided.

4.5 Environmental Specifications of DXX Products

4.5.1 Safety compatibility

Basic and Cluster Node	EN60950:1992 (A1:1993; A2:1993)
Midi Node Tabletop	EN60950:1992 (A1:1993; A2:1993; A3:1995)

4.5.2 Climatic/Mechanical Compatibility

	Storage	**Transport**	**In use**
Basic and Cluster Node	ETS 300 019-1-1:1992-02 Class1.1 Weatherprotected, partly temperature controlled storage locations -5...+45°C	ETS 300 019-1-2:1992-02 Class2.3 Public transportation -25...+70°C Note:Rain is not allowed; -25 °C maximum	ETS 300 019-1-3:1992-02 Class 3.1 +5...+40°C (--5...+45°C)
Midi Node Tabletop	ETS 300 019-1-1:1992-02 Class1.1 Weatherprotected, partly temperature controlled storage locations -5...+45°C	ETS 300 019-1-2:1992-02 Class2.3 Public transportation -25...+70°C Note:Rain is not allowed; -25 °C maximum	ETS 300 019-1-7:1992-02 Class 7.1 +5...+40°C

4.5.3 Electromagnetic compatibility

EMC

	EMC
Basic and Cluster Node, Midi Node (rack mounted)	ETS 300386-1: 1994-12 Table2 Table4 in EMC cabinet Surge test compliance criteria for indoor signals is LFS (ITU-T Rec. K.21)
Midi Node Tabletop	ETS 300386-1: 1994-12 Table4 At AC input only for table4; table 2 for DC input (EFT test) Surge test compliance criteria for indoor signals is LFS (ITU-T Rec. K.21)

4.5.3.1 General

The electromagnetic environment varies from time to time and from place to place in a very complicated manner. The concept of environmental classes for climatic and mechanical environments introduced by the IEC, and implemented by ETSI, takes these aspects into account.

An environmental class refers to the environments encountered in a group of locations with similar properties. ETS 300 386-1 defines electromagnetic environmental classes for public telecommunication equipment:

- telecommunication centres, classes 1 and 2
- locations other than telecommunication centres, classes 3 and 4

ETS 300 386-1 also specifies all parameters that are not specific to a particular equipment. These are:

- general operating conditions
- test levels for immunity (tables 2, 3, 4 and 5) and associated general compliance criteria. Test levels are specified according to environmental class and according to priority of service.
- emission limits related to an environmental class

Compliance criteria for immunity tests:

- Normal performance
- Reduced performance
- Loss of function

To fulfill the requirements, DXX nodes should be installed to cabinets that are appropriate to stated installation category. In telecommunication centres the installation may be done by using standard cabinets like RSR 124 (43HE standard 19” cabinet); by doing so the installation meets test levels specified in table 2 (telecommunication centres, normal priority of service). In table 4 the test levels (other than telecommunication centres, normal priority of service) require that the installation is made by using EMC cabinet RSR122 (43HE EMC cabinet).

NOTE! ***Unused unit positions must be covered with 5T cover plates to fulfill the EMC requirements.***

4.5.3.2 DXX performance criteria for continuous interference:

Normal Performance (NP) within specified limits

The EUT shall withstand the applied test without damage. No degradation of performance is allowed (Bit Error Rate better than 10E-9). In the Electrostatic Discharge test occasional Bit Errors are allowed. Corruption of any software or data associated with the EUT is not permitted. This includes data stored in memory or data in process within the EUT (i.e. loss of system settings or cross-connections).

Reduced Performance (RP)

- The EUT shall withstand the applied test without damage
- Corruption of software or data held in memory shall not occur (i.e. loss of system settings or cross-connections)
- Reduced performance is permitted within specified relaxed limits (BER < 10E-4)
- AIS (Alarm Indication Signal) must not be generated to the operating interfaces
- resumption to normal performance shall occur at cessation of the test

Loss of Function (LFS), self recovery

- The EUT shall withstand the applied test without damage
- Corruption of software or data held in memory shall not occur
- Temporary loss of function following application of test is permitted (i.e. signal to operating interface may be interrupted)
- AIS (Alarm Indication Signal) can be generated to the operating interfaces
- self recovery to normal performance shall occur at cessation of the test

Loss of Function (LFC), Customer reset

Not applicable; should not happen within tested values

Loss of Function (LFO), Operator reset

Not applicable; should not happen within tested values

4.5.3.3 DXX Products Usage Limitations

- GDH 230, G703 (G.703 2Mbit/s, 8Mbit/s) module should always be installed in EMC cabinet when 8 Mbit/s is used.
- BTE-64 nor BTE-384 (version 2.0 or earlier) does not fulfill the test level 1 of ENV 50141 (1993), Conducted Disturbances Induced by Radio Frequency Fields; Immunity Test.

Appendix: Midi Node G.704 Frame Structures

2048 kbit/s Frame Structure

The DXX system utilizes a frame structure for 2048 kbit/s according to G.704. The first time slot of a frame, ts0, contains the Frame Synchronization Word (FSW). The bits of this frame synchronization word have a different meaning in odd and even frames. Even frames contain the frame alignment signal and odd frames specify one bit of this word as a frame alignment signal, one bit as the far-end alarm bit and five special bits. Four of these five special bits are recommended to be used for the internal HDLC channel of the DXX system. The function of these bits is defined in the user interface through the GDH (interface) Parameterization window. However, if CRC check is used, then the first bit in time slot ts0 of every frame is used by the CRC check and cannot be defined for other purposes in the user interface.

The first bit of 16 consecutive time slots ts0 form a CRC multiframe consisting of 16 frames. This multiframe has six frame synchronization bits, eight bits for the CRC check sum, and two bits used to transmit far-end block error information. The period of 16 frames is divided into two subgroups, each consisting of eight frames. A check sum is separately calculated for both subgroups and sent during the next subgroup. The receiving end performs the CRC check, and if a faulty block is detected, then information about this is sent to the far-end by setting the corresponding block error bit to state 0 during one multiframe.

Time slots ts1…ts15 and ts17…ts31 are reserved for payload data transmission. Each data time slot has a corresponding 4-bit signalling word, which is transmitted in time slot ts16 of a multiframe. The bits in time slot ts16 can be utilized by other functions if no signalling capacity is required by a data time slot.

The length of a multiframe is 16 frames. Within the multiframe the first ts16 time slot (in the first frame) is used to transmit the multiframe synchronization word (four bits in the 0 state), the multiframe far-end alarm and three special bits. The function of the special bits can be defined through the user interface. It is recommended to set these bits in state 1 when they are not used. The ts16 time slots of the other frames carry signalling data for two time slots each, four bits for each data time slot. For example, ts16/Fr1 carries signalling data for the time slots ts1 and ts17.

An HDLC channel can be placed in any free time slot where it can occupy a required number of bits. A time slot bit can carry 8 kbit/s of data, and thus the total capacity of the 8 bits in a time slot is 8 x 8 = 64 kbit/s. It is, however, recommended to locate the HDLC channel in the bits B5, B6, B7 and B8 of the time slot ts0. Due to the frame alternation the time slot TS0 capacity is only 4 kbit/s per bit, and these four bits together provide a 16 kbit/s transmission channel. If the HDLC channel is located in bit B1 of time slot ts0, replacing the CRC check, then no other bits can be used to form the HDLC channel.

Frame Multiplexing and Demultiplexing at 2048 kbit/s

A frame to be transmitted is multiplexed in the Frame Mux and clocked by the Tx clock. The data to be transmitted is received through the X-bus into a transmit buffer, from which the Frame Mux fetches data, one time slot at a time, controlled by the bus frame clock. The time slot ts0 can also be received via the transmit buffer from the bus, but usually the frame alignment signal is generated in the Mux. The other bits for the ts0 are read into the transmitted frame from positions defined through the user interface. E.g. the HDLC channel data is received from the HDLC controller in serial form and clocked by the Tx clock. The data for the first frame in the signalling multiframe is generated in the Mux and the time slot signalling data is received via the transmit buffer from the X-bus. Before the frame is transmitted, a CRC check sum is calculated and the CRC multiframe structure is placed into the first bit of time slot ts0.

The receiver will search for the frame alignment signal in the received decoded signal. When the alignment is found at the correct position in consecutive frames, the receiver is synchronized and the frame demultiplexed. The frame alignment search is performed in accordance with a state diagram which should ensure that the receiver will be correctly synchronized even on noisy connections.

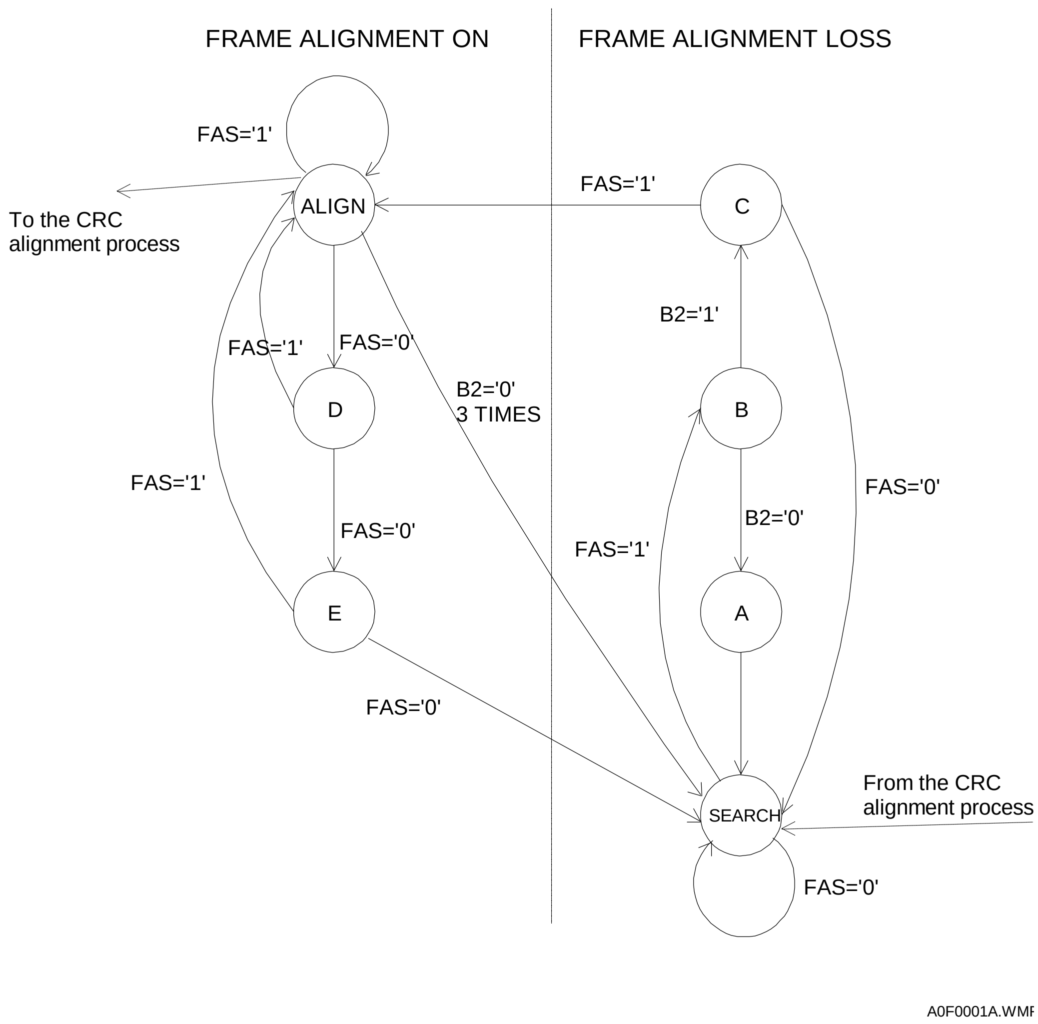

Fig. 40: Frame Alignment State Diagram at 2048 kbit/s

The right-hand side of shows the states in the search mode: the frame alignment alarm is activated and the data to the X-bus is set to AIS. On the left-hand side the receiver is synchronized to a received frame and the alarm is inactive. In the search mode the correct frame synchronization word must be found, thereafter the time slot ts0 in the next frame must have the bit B2 in state 1, then the frame synchronization word again has to be in the correct position in the next frame, and only then the frame is synchronized. If any of these conditions is not fulfilled, the search is repeated from the beginning. When the frame is synchronized, the frame alarm is inactivated and at the same time the AIS is removed from the data supplied to the X-bus.

When the frame alignment is found, the receiver monitors the received frame synchronization words. The frame alignment is considered lost if a corrupted frame synchronization word is received in three consecutive frames. In this case the frame synchronization alarm is activated and a new frame alignment search is started. The receiver monitors also the state of bit B2 in time slot ts0 of odd frames. The frame alignment is considered lost if the bit B2 is 0 in three consecutive frames.

The number of faulty frame synchronization words is also counted in the receiver in order to calculate the error rate of the connection. Normally, the error rate limit is set to 10E-3. If the error rate exceeds this value, the reception is inhibited and the receiver sets AIS as data to the X-bus and activates the error rate alarm. The error rate is not calculated when the frame alignment is lost.

The state of the received data bits is monitored in order to detect an AIS. The received data is considered to be AIS if there are less than three bits in state 0 during two frames and a corresponding alarm is activated. The far-end alarm bit is extracted from time slot ts0 in a received frame. The alarm bit is filtered so that three identical states in consecutive frames are required to change the filtered value. A filtered value 1 activates the functions defined in the alarm table.

In receiver fault situations - if the error rate is too high or if the frame alignment is lost, for instance - the receiver transfers corresponding information to the transmitter which then activates the far-end alarm bit in the transmitted time slot ts0.

The CRC check is used to increase the reliability of frame alignment and to prevent alignment on words only simulating the frame synchronization word. The receiver is synchronized to the first word found to be identical with the frame synchronization word. If this detected word is sent by some data equipment in a data slot and if this word remains the same for a longer period, the receiver can falsely synchronize to this simulating synchronization word. This situation is detected with the CRC check.

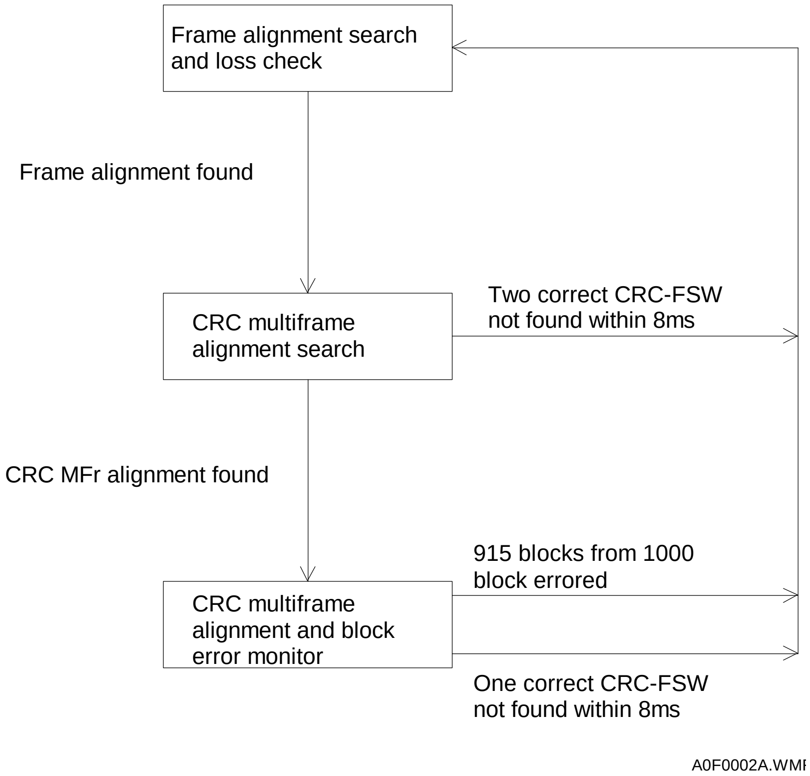

Fig. 41: CRC Multiframe Alignment State Diagram at 2048 kbit/s

The CRC multiframe alignment state diagram is shown in. The state at the top contains the 2048 kbit/s frame alignment state diagram. When frame alignment is found, the receiver starts the search for the CRC multiframe alignment signal. The CRC multiframe alignment is found when the receiver finds two correct CRC multiframe alignment signals in the correct position within a period of 8 ms. Then the CRC error count is started. If two CRC multiframe alignment signals are not found within the period of 8 ms, then also a new frame alignment search is started and a frame synchronization alarm is activated.

The receiver starts to count CRC block errors when the CRC multiframe alignment is found. The frame alignment search is started and an alarm is activated if there are more than 914 faulty blocks out of 1000 blocks. The CRC multiframe synchronization words are also monitored: if no correct CRC multiframe synchronization word is found within 8 ms, then a new frame alignment search is started.

The signalling multiframe consists of the time slots ts16 of 16 consecutive frames. The first four bits of time slot ts16 in the first frame form the multiframe synchronization word. These bits are all zeroes (0). The other time slots ts16 contain signalling information for the data time slots.

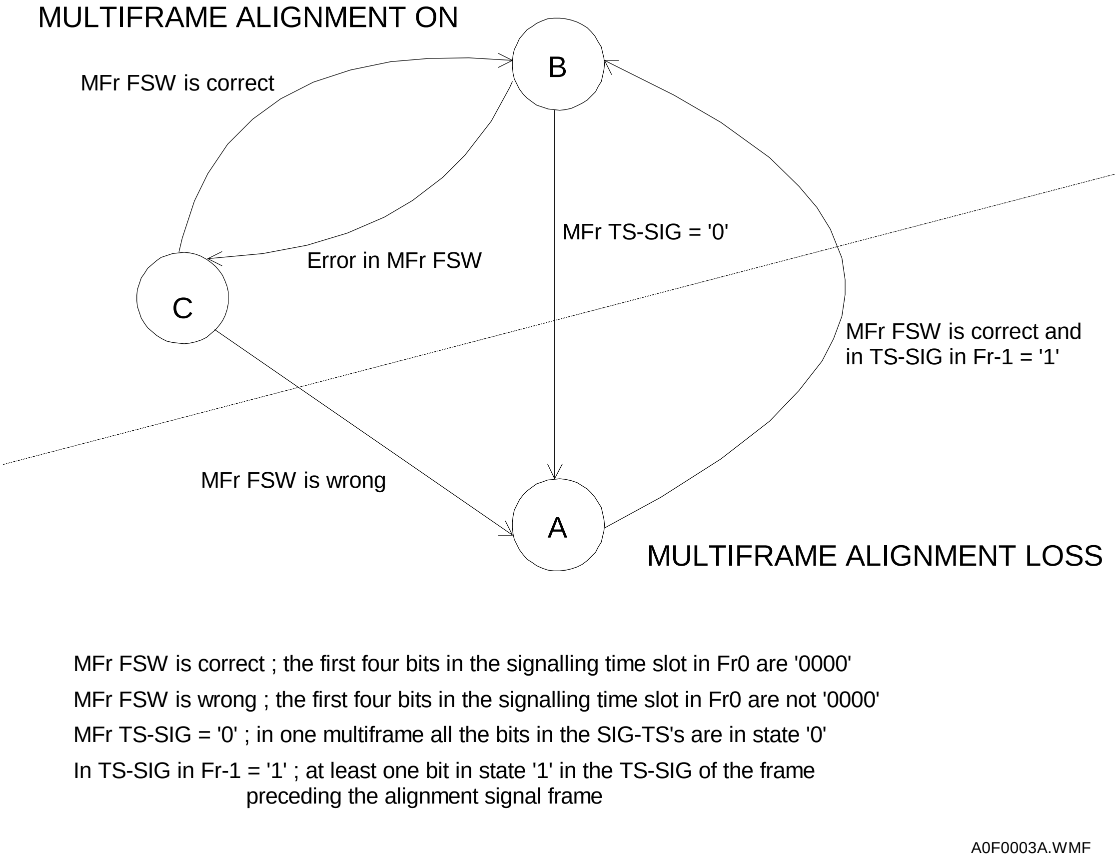

Fig. 42: Signalling Multiframe Alignment State Diagram

The signalling multiframe alignment signal search begins when the frame alignment is found. When the first four bits of time slot ts16 are found to be zeroes (0), this is considered to be the multiframe synchronization word. However, in order to avoid a false alignment it is required that the prior time slot ts16 had at least one bit in state 1. The AIS is removed from the signalling information to the X-bus and the multiframe alarm sent to the far-end is inactivated when the alignment is found.

The multiframe synchronization word monitoring function is started when the multiframe is synchronized. If errors are found in two consecutive synchronization words, the multiframe alignment is considered to be lost. In the synchronized state the contents of all time slots ts16 are monitored, and if all time slots ts16 in one multiframe contain only zeroes (0) the multiframe alignment is considered to be lost. A corresponding alarm is activated if the alignment is lost, the signalling data to the X-bus is set to AIS and the transmitted far-end alarm is activated (ts16/B6).

The far-end alarm is extracted from the received signalling multiframe synchronization time slot. The alarm state is filtered so that three identical states in consecutive frames are required to change the filtered value. A filtered value 1 activates an alarm. Through the user interface it is possible to define that the alarm state also puts the signalling data to the X-bus to AIS. In such case the frame far-end alarm bit will also put the signalling data directed to the X-bus to AIS.

If the signalling multiframe synchronization is lost, the received signalling time slot data is monitored in order to detect an AIS. A signal is considered to be AIS if the signalling time slot during one multiframe contains only one bit or no bits in state 0.

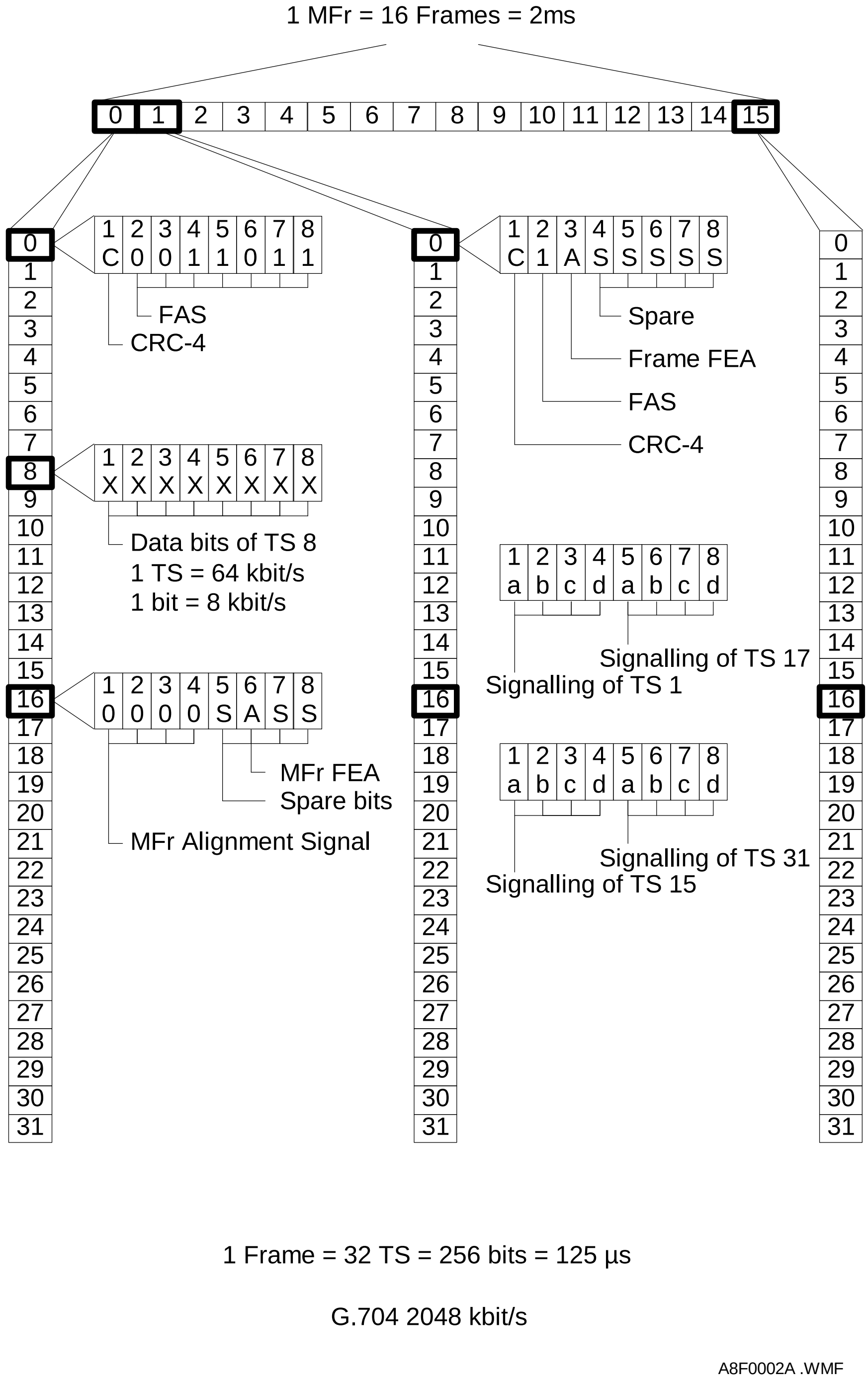

Fig. 43: 2048 kbit/s Frame Structure

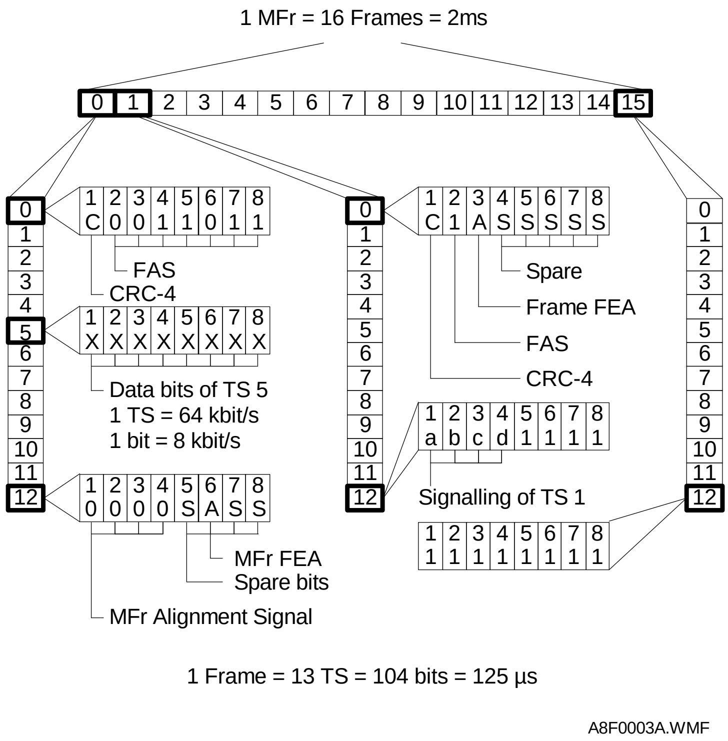

Fig. 44: N x 64 kbit/s Frame Structure

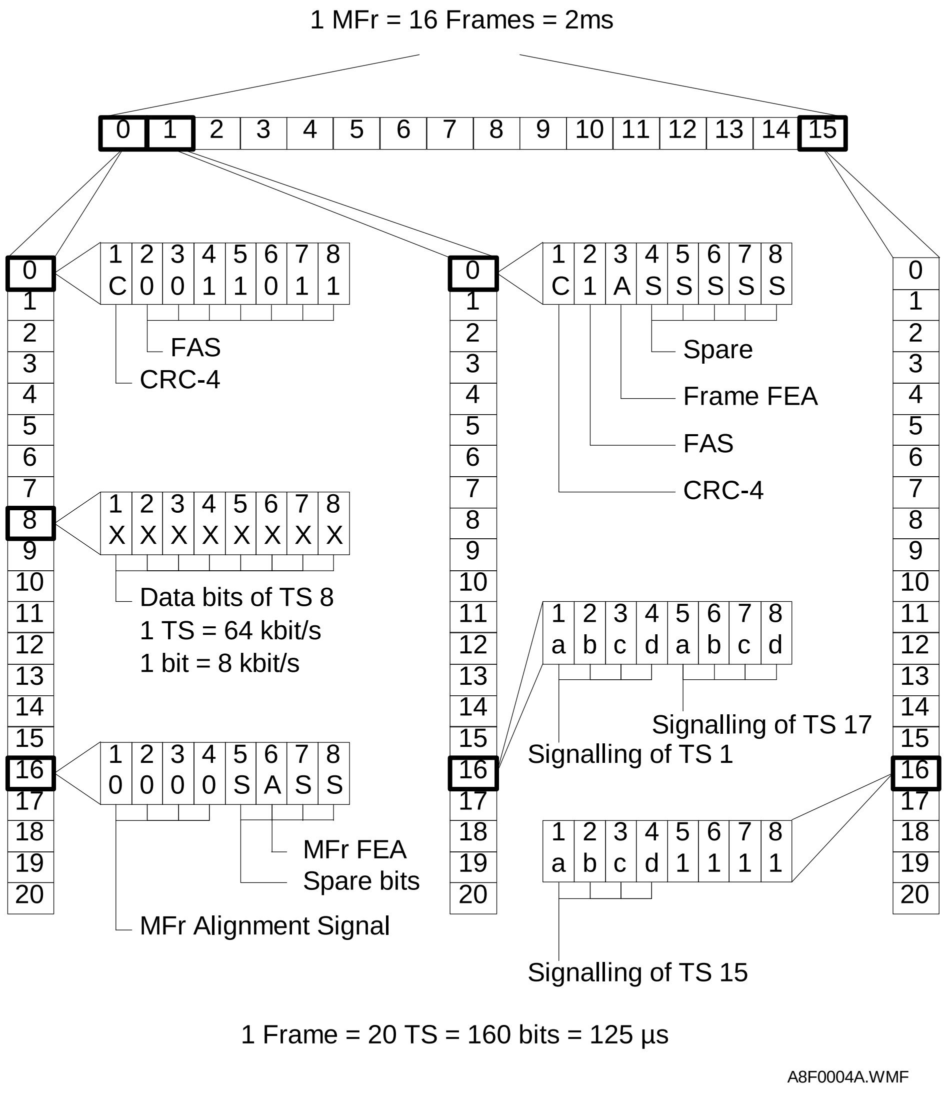

Fig. 45: N x 64 kbit/s Frame Structure

Multiframe Structure in the Signalling Time Slot

2 Mbit/s frame and n x 64 kbit/s frame with n >17 ts16. N x 64 kbit/s frame with n≤17 tsn-1.

[a]Frame #	Sigtsbits 1234 abcd	Sigtsbits 5678 abcd	Use
0	0000	SASS	0000=M-FSW, A=FEA (1-active), S=spare
1	ts1	ts17	abcd bits for ts1 and ts17 of the group
2	ts2	ts18	
3	ts3	ts19	
4	ts4	ts20	
5	ts5	ts21	
6	ts6	ts22	
7	ts7	ts23	
8	ts8	ts24	
9	ts9	ts25	
10	ts10	ts26	
11	ts11	ts27	
12	ts12	ts28	
13	ts13	ts29	
14	ts14	ts30	
15	ts15	ts31	abcd bits for ts15 and ts31 of the group

a Multiframe length is 16 frames/125 µs = 2 ms (500 Hz)

CRC Multiframe Structure in ts0 for the 2 Mbit/s and n x 64 kbit/s Frames

Frame #	**ts0 bits** **1**	**2345678**	**Use**
Block #1			
0	C1	0011011	C1…C4 = [a] CRC-4 bits
1	0	1ASHHHH	A = FEA (1-active), S = spare
2	C2	0011011	0011011 = FSW, H = reserved for the HDLC link
3	0	1ASHHHH	001011 = CRC M-FSW
4	C3	0011011	
5	1	1ASHHHH	
6	C4	0011011	
7	0	1ASHHHH	
Block #2			
8	C1	0011011	
9	1	1ASHHHH	
10	C2	0011011	
11	1	1ASHHHH	
12	C3	0011011	
13	E1	1ASHHHH	E1 = BlockI FEA (0-active)
14	C4	0011011	
15	E2	1ASHHHH	E2 = BlockII FEA (0-active)

a The CRC multiframe length is 16 frames/125 µs = 2 ms (500Hz).